Direct Conversion RF Front-End Implementation for Ultra-Wideband (UWB) and GSM/WCDMA Dual-Band Applications in Silicon-Based Technologies

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Direct Conversion RF Front-End Implementation for Ultra-Wideband (UWB) and GSM/WCDMA Dual-Band Applications in Silicon-Based Technologies

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Table of Contents

List of Tables

List of Figures

Summary

This dissertation focuses on wideband circuit design and implementation issues up to 10GHz based on the direct conversion architecture in the CMOS and SiGe BiCMOS technologies. The dissertation consists of two parts: One, implementation of a RF front-end receiver for an ultra-wideband system and, two, implementation of a local oscillation (LO) signal for a GSM/WCDMA multiband application. For emerging ultra-wideband (UWB) applications, the key active components in the RF front-end receiver were designed and implemented in 0.18um SiGe BiCMOS process. Both the DS-CDMA system and the MB-OFDM system are discussed from the perspective of implementation issues for the FCC-allowed UWB system. The design of LNA, which is the critical circuit block for both systems, was analyzed in terms of noise, linearity and group delay variation over an extemely wide bandwidth. Measurements are demonstrated for an energy-thrifty UWB receiver based on an MB-OFDM system covering the full FCC-allowed UWB frequency range.

For multiband applications such as a GSM/WCDMA dual-band application, the design of wideband VCO and various frequency generation blocks are investigated as alternatives for implementation of direct conversion architecture in a standard CMOS process in which thin metal lines and low resistive substrates limit the quality factor achievable in the passive components. Two 4GHz wideband CMOS VCOs were designed and implemented to assess and compare their phase-noise performance over a wide tuning range.

In order to reduce DC-offset and LO pulling phenomena that degrade performance in a typical direct conversion scheme, an innovative fractional LO signal generator was designed and implemented in a standard CMOS process. A simple analysis is provided for the loop dynamics and operating range of the design as well as for the measured results of the factional LO signal generator.

CHAPTER I

INTRODUCTION

1.1 TECHNOLOGY TRENDS

The explosive growth of commercial wireless communications has been driven mainly by consumer demand for enhanced functionality in smaller and more affordable handsets and handhelds and for high-speed wireless data services. Wireless voice communication systems began in the early 1960s and now wireless systems pervade everything in our daily life. This enormous growth has been driven by three main criteria: (i) a higher data rate, (ii) enhanced user convenience, and (iii) lower cost. In the early days of wireless communication systems, reliable voice communication was the ultimate goal in system design. However, the success of wireless communication systems in the late twentieth century has transformed the design goal and redirected it toward replacing wired systems in every possible situation. A simple example would be a mouse with Bluetooth capability that does not require a cord to connect it to a computer. This goal of a wireless environment inevitably extends to a concept of ubiquity, which in terms of wireless communication can be defined simply as "anywhere at any time". In a ubiquitous environment, communication devices will interact with each other seamlessly and users will use a simple platform to obtain information at any time without any awareness of a distinction between wireless and wired networks. To create this ubiquitous environment, future wireless communication systems will be characterized by a horizontal communication model to access different technologies such as cellular, cordless, wireless local area network (WLAN)-type systems, short-range connectivity and broadcast

systems. These technologies will be integrated on a common platform in such as way as to optimally complement each other and to satisfy different service requirements in a variety of radio environments.

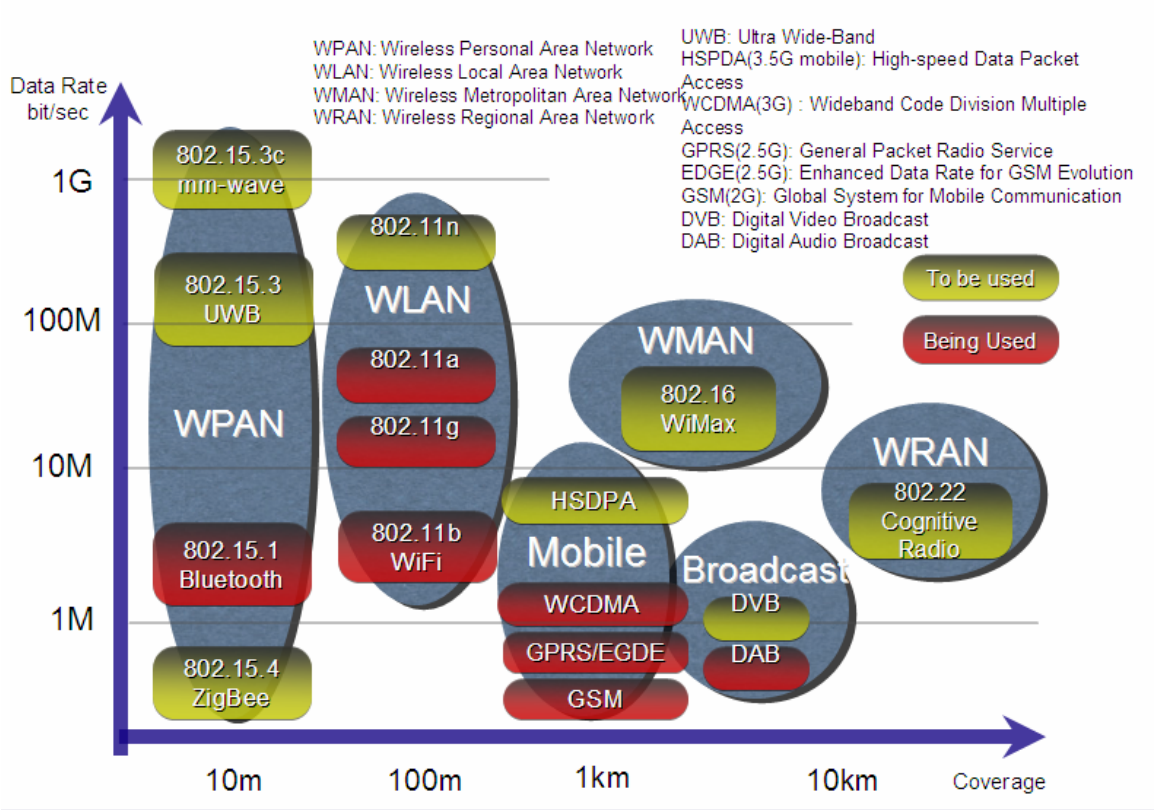


Figure 1.1 Various wireless systems along with data rates and distances

Signs of movement in the direction of a common platform can be seen in efforts to integrate GSM and WCDMA communication system into one chip solution and to add Bluetooth functionality in an existing cellular phone. Figure 1.1 shows currently developed or developing wireless communication systems. Various systems serve distinct purposes. For instance, a Zigbee application aims to deliver data at a very low rate but with extremely little power consumption. The application is suitable when the lifetime of

a battery is important and the low data rate is nevertheless enough to serve its purpose.. On the other hand, mobile systems such as WCDMA aim at reliable voice communication and proper data service over long distances. In the end, these various systems will be integrated into a single platform satisfying the various needs of users.

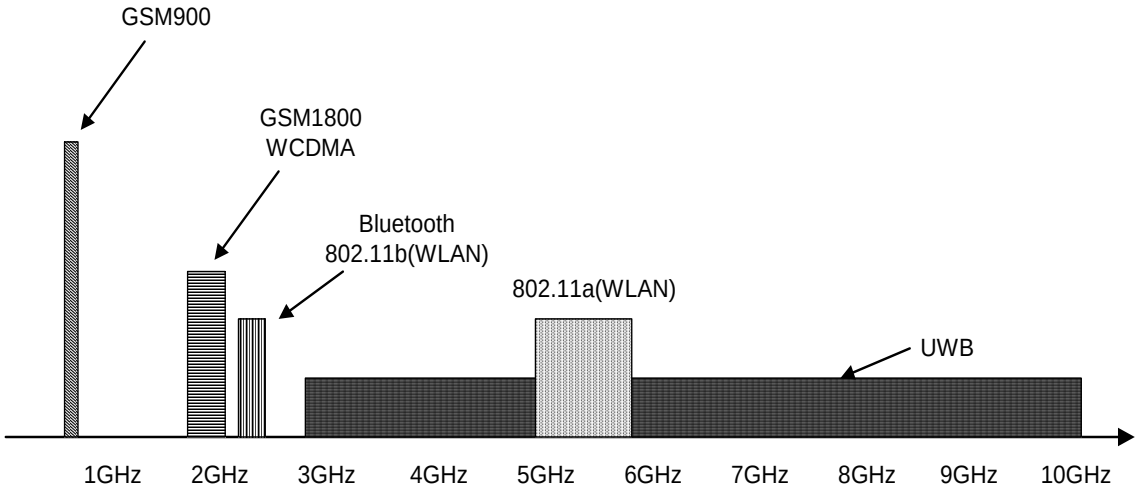


Figure 1.2 Allotted spectrum of various applications

Figure 1.2 shows the allotted spectrum for wireless applications. Each application occupies a different frequency range. This traditional approach of assigning a specific narrow frequency range to each type of system poses challenges to the integration of these systems on a common platform.. From an implementation point of view, RF front-ends support these various systems in the simplest way possible to reduce implementation cost; this suggests that the active as well as the passive components of RF- front-ends should cover the required wide frequency ranges while simultaneously satisfying the specifications of the different standards.

Moreover, the recent allowance of the FCC regarding frequencies between 3GHz and 10GHz for UWB applications has brought this frequency band and its various applications an increased level of interest and broadened the scope of research devoted to it. The availability of such high bandwidth would allow higher data throughput up to 500Mbps over short distances, which is desirable for HDTV and other wireless multimedia applications. Apart from high data rates, the other compelling features of UWB would be potentially lower cost and higher levels of integration.

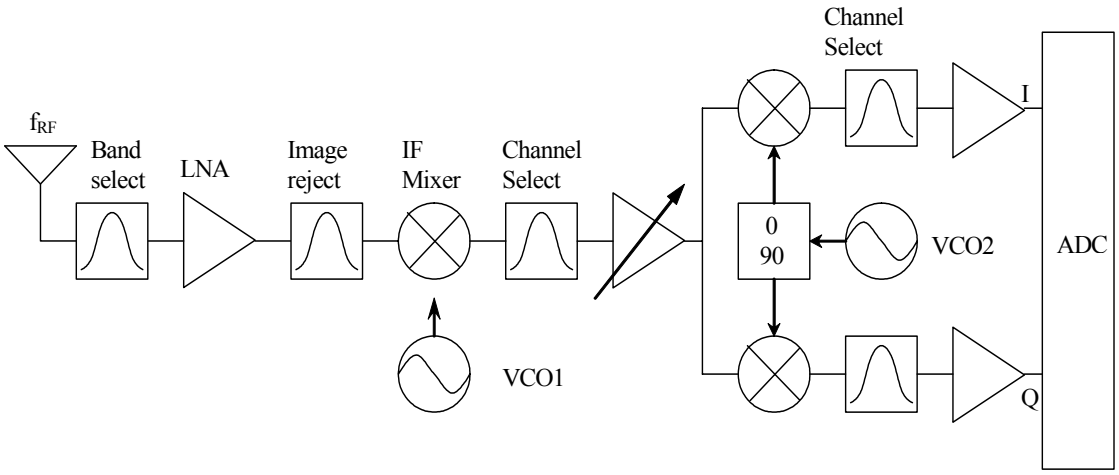
To catch up with these trends and provide a cheap solution in a timely manner, the issues in implementing the RF front-end for wideband applications such as a UWB system and a multiband, multimode system need to be investigated.

1.2 MOTIVATION FOR DISSERTATION

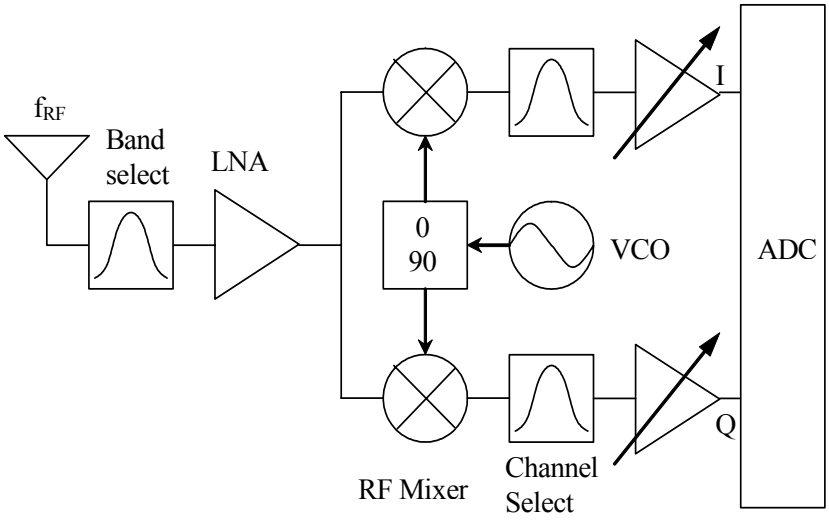
Since the day Armstrong invented the superheterodyne RF front-end architecture, it has been widely used in implementing RF circuitry for wireless communication systems. Because of the expensive external components and complex frequency planning in the design of superheterodyne architecture, direct conversion architecture has been a major research focus for several years. Future technical advances may make feasible a software-defined-radio in which a RF analog digital converter (ADC) replaces most of the RF circuitry. However, such a radio is impractical at present because of limitations such as high power consumption, limited dynamic range, high frequency operation and poor noise performance. These architectures are shown in Figure 1.3.

The direct conversion scheme has been an active research topic for several years because it is capable of implementing systems with reduced cost and complexity. Its simple architecture enables wireless communication systems to integrate into a single-

chip solution. However, the direct conversion scheme suffers from drawbacks such as flicker noise, DC-offset, IIP2, LO radiation, and I/Q mismatches. These problems become severe when the architecture is implemented in a silicon based-technology such as a CMOS process.

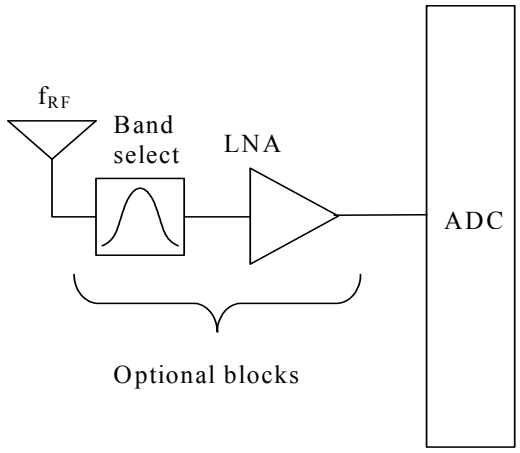


(a) Superheterodyne



(b) Homodyne/direct conversion

Figure 1.3 RF receiver architecture for superheterodyne, direct conversion, software-defined-radio



(c) Software-defined radio

Figure 1.3 RF receiver architecture for superheterodyne, direct conversion, software-defined-radio

Even though III-V semiconductors such as GaAs HBT or pHEMT provide better performance in terms of their power handling capability, insulation and noise, the main thrust that drives the commercial communication market is the capability of realizing a low- cost system on a single chip (SOC), which is not provided by III-V semiconductors. Since most of the digital circuitry is designed using a silicon-based process, CMOS or SiGe HBT BiCMOS technologies are the most attractive design platforms to implement RF front-ends.

In addition to the problems arising because of the system architecture and semiconductor technologies, the emerging UWB applications and the current trends of multiband, multimode operation have created even more challenges. A major reason that silicon-based technologies have been successfully used in the implementation of RF front-ends is that a relatively high quality factor inductor can be built in the process by using a thick top metal. Resonating techniques that have been widely used in traditional

narrow band RF circuit design use passive components such as inductors and capacitors. However, inductors and capacitors are frequency dependent components, which means that the magnitude and phase of their impedance varies along with the frequency. Because of the frequency dependent characteristics of the passive components, the design of a wideband RF circuit becomes difficult, and it tends to occupy more space and consume more DC power [6].

The objective of the research in this dissertation is to investigate issues in silicon-based technologies in the implementation of the direct conversion receiver for wideband applications such as UWB system and a multiband GSM/WCDMA system. Since the design of the receiver is targeted at such wideband applications, the research mainly focuses on achieving a wideband operation while meeting the specifications of the system with minimized DC power consumption. For this purpose, each RF block of the direct conversion receiver is investigated. The contributions of this research will be as follows:

1. The design considerations for the implementation of the UWB RF front-end will investigated based on the system architecture. The key design parameters for the UWB receiver will be identified.

2. The design and concept behind a wideband LNA will be demonstrated with detailed analysis of group delay variation, noise figure, and linearity.

3. A low DC power consuming UWB direct conversion receiver will be presented.

4. Critical performance degradation in a wideband VCO will be identified and demonstrated.

5. A proposed solution will be provided to solve the LO signal generation issue in a

multiband, multimode direct conversion receiver. The concept of the fractional signal generator is analyzed and demonstrated.

1.3 ORGANIZATION OF DISSERTATION

This dissertation consists of two contributions. First, the direct conversion receiver implementation of an ultra-wideband RF front-end will be discussed, and the measured results will be demonstrated. Second, the LO signal generation implementation for the GSM/WCDM multiband application will be presented. Although the concept of using ultra-wide bandwidth is old, the idea of a UWB system designed to deliver data at a high rate over a short distance with noise-like power spectrum density has emerged only since February 14, 2002, when the FCC opened up 7,500 MHz of spectrum for use by UWB devices. Therefore, Chapter Two provides an overview of the FCC-allowed UWB system. In this chapter, restrictions imposed by the FCC are discussed. The proposed approaches to realize UWB systems by wireless companies are illustrated and reviewed from the perspective of implementation issues. Key building blocks in the RF UWB receiver are identified. Chapter three provides a detailed analysis of the UWB LNA design. The technical analysis includes wideband input matching, noise performance, linearity issues, and group delay variation over the entire UWB band. A theory has been developed to control the group delay variation of the LNA. Simulation and measured results of the designed LNA in 0.18um SiGe BiCMOS process are reported and compared. Chapter Four presents a direct conversion implementation of a UWB receiver in a 0.18um SiGe BiCMOS process based on the UWB multiband OFDM (MB-OFDM) approach. The UWB MB-OFDM system is discussed in more detail. Challenges in the conventional narrowband direct conversion architecture are reviewed in conjunction with the issues of

the implementation of a direct conversion UWB receiver. Chapter Five shows the investigation of a CMOS VCO design for a wide frequency tuning range and low phase noise. The basic theory of the phase noise of an oscillator is described, and the impact of phase noise on a system is illustrated. The measured results of two CMOS VCOS are compared in terms of tuning range and phase noise. Chapter Six introduces a CMOS fractional LO signal generator to solve the issues in direct conversion architecture. Operational principles of the design are explained with qualitative analysis. The performance of the signal generator is demonstrated for the GSM/WCDMA dual band application. Finally, Chapter Seven concludes the dissertation with a discussion on potential future work.

CHAPTER II

OVERVIEW OF ULTRA-WIDEBAND SYSTEM

2.1 THE HISTORY OF ULTRA-WIDEBAND

When radio was invented by Guglielmo Marconi more than a century ago, radio communications used enormous bandwidth in the course of conveying information by using spark-gap transmitters. The next milestone of UWB technology came in the late 1960s, when UWB radar systems were introduced in the search for high sensitivity to scatterers and low power consumption. Since Armstrong's invention of heterodyne techniques, most RF transceivers have switched over to narrowband approaches. As a result, until recently UWB technology has been used mostly for radar-based applications because the wideband nature of the signal results in very accurate timing information. However, recent developments in high-speed switching technology have made UWB more attractive for low-cost consumer communications applications [7].

2.2 FCC-ALLOWED UWB SYSTEM

The UWB system discussed in this thesis differs from what has traditionally been called an ultra-wideband system that can best be understood as impulse radio. Recently, the Federal Communications Commission (FCC) allowed a wide frequency spectrum of 3.1-10.6GHz to be used for a communication system as long as the new system does not degrade the performance of previously existing communication systems. The huge "new bandwidth" opens the door for an unprecedented number of bandwidth-demanding position-critical low-power applications in wireless communications, networking, radar

imaging, and localization systems [7]. Among the many possible applications for the newly allowed UWB spectrum, this thesis will focus on approaches to implement wireless communication systems based on the FCC's definition of what constitutes a UWB system

2.2.1 Definition of UWB

Traditionally, UWB technology has been loosely defined as any wireless transmission scheme that occupies a bandwidth of more than 25% of a center frequency, or more than 1.5GHz. Clearly, this bandwidth is much greater than the bandwidth used by any current technology for communication. More recently the FCC [8] has defined a UWB device as one with fractional bandwidths greater than 20% or one that occupies at least 500MHz of spectrum. Furthermore, the FCC has regulated the spectral shape and maximum power spectral density of UWB radiation in order to limit interference with other systems, as shown in Figure 2.1.

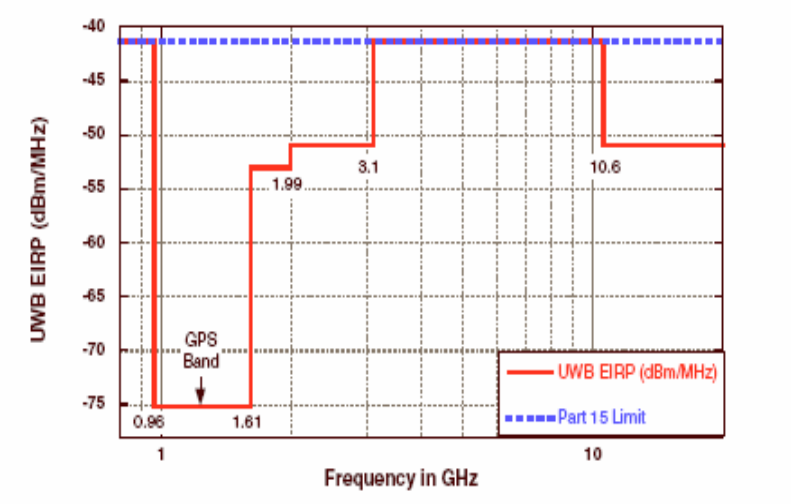


Figure.2.1 FCC spectral mask for indoor UWB systems.

2.2.2 Power emission

The FCC's Part 15 rules [8] place emission limits on intentional and unintentional radiators in unlicensed bands. These emission limits are defined in terms of microvolts per meter (uV/m), which represent the electric field strength of the radiator. In order to express this in terms of radiated power, the following formula can be used. The emitted power from a radiator is given by the following:

$$P = \frac{E_o^2 4\pi R^2}{\eta} \qquad (2.1)$$

Where E_o represents the electric field strength in terms of *V/m*, *R* is the radius of the sphere at which the field strength is measured, and η is the characteristic impedance of a vaccum in which η =377 ohms. For example, for frequencies greater than 960MHz, the FCC's Part 15 rules limit emissions of intentional radiators to 500uV/m measured at a distance of three meters in a 1MHz bandwidth. This corresponds to an emitted power spectral density of -41.3dBm/MHz.

2.2.3 Channel capacity

Part of the interest in UWB systems is prompted by considering the Shannon's channel capacity theorem in Eqn. 2.2.

$$C = B\log_2\left(1+\frac{S}{N}\right) \qquad (2.2)$$

Where

C=Maximum channel capacity (bits/sec)

B= Channel bandwidth (Hz)

S= Signal power (watts)

N= Noise power (watts)

Eqn. 2.2 shows that capacity increases linearly with bandwidth but only logarithmically with an increasing signal-to-noise ratio (SNR). Shannon's theorem suggests maximum channel capacity. If the actual desired capacity (R) is not too close to C and/or the bit error rate (BER) is not too low, then in theory the transceiver design is simpler. However, as we approach channel capacity, more complex coding and modulation techniques must be used to gain the desired channel throughput. Therefore, having a larger bandwidth available allows for significantly lower RF transmit power while still accommodating large channel throughput. Because the upper boundary of channel capacity increases linearly with total available bandwidth, UWB systems have more room for expansion than systems that are more constrained by bandwidth.

2.2.4 Coexistence with the existing wireless systems

Because a UWB device spreads its signal energy over a large frequency range, it only radiates a small percentage of its total power in the operating spectrum of narrowband applications such as global positioning systems (GPS), federal aviation systems (FAS), and WLAN. Hence, UWB signals should appear as low-power white noise and have little impact on underlying operating devices. To regulate coexistence of UWB signals and other existing systems, the FCC has released a spectral mask that limits the equivalent isotropic radiated power (EIRP) spectrum density with which UWB radios are allowed to transmit. It has thus been asserted that UWB devices, with appropriate restrictions on effective radiated power (ERP), can coexist with other devices in the same

frequency band without causing interference, thereby making efficient use of already scarce spectrum. To ensure this, the FCC has defined the UWB power mask so as to allow only a maximum transmitted spectral density (PSD) of -41.3dBm/MHz. A myriad of potential interferers operate in the spectrum allotted for UWB use, as can be seen in Figure 2.2 [9,10,11].

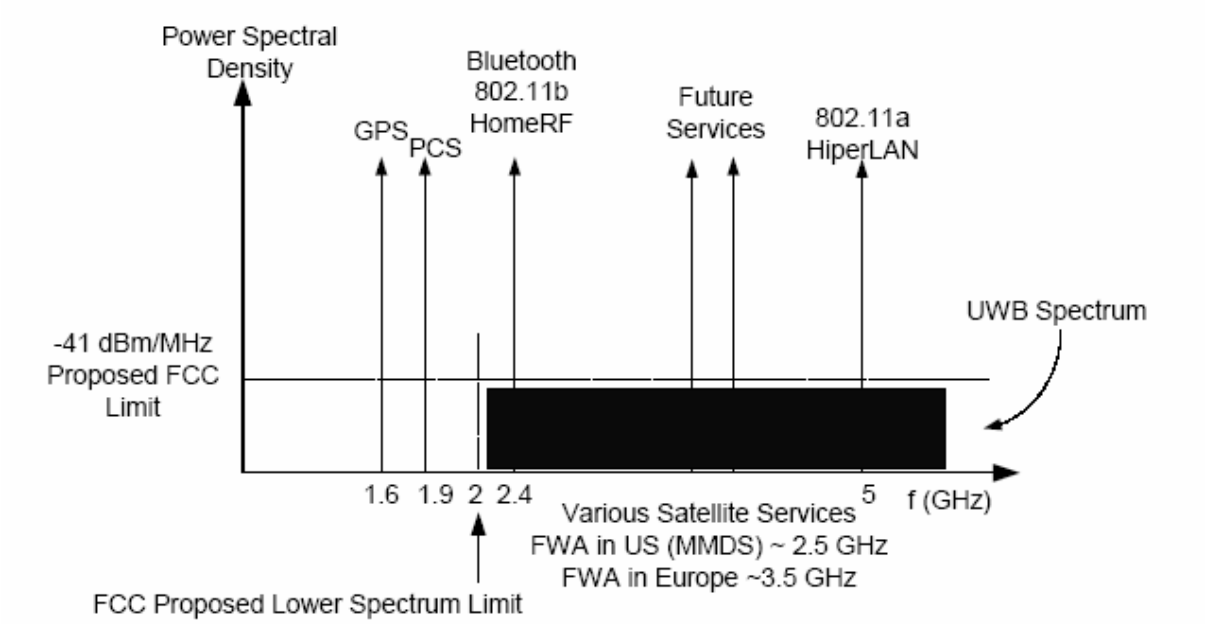


Figure 2.2 Potential interferers for a FCC-allowed UWB system

2.2.5 UWB target applications

The huge new bandwidth opens the door for an unprecedented number of bandwidth-demanding position-critical low-power applications in wireless communications, networking, radar imaging, and localization systems [7]. It also

expedites the potential for the use of UWB radios in short-range, high-speed access to the Internet and in such applications as accurate personnel and asset tracking for increased safety and security, precision navigation, imaging of steel reinforcement bars in concrete or detection of pipes hidden inside walls, surveillance, and medical monitoring of the heart's actual contractions.

For wireless communications in particular, the FCC-regulated power levels are very low, which allows UWB technology to overlay already available services such as the GPS and the EEE 802.11 wireless local area networks (WLANs) that coexist in the 3.1-10.6 GHz band. Although UWB signals can propagate for greater distances at higher power levels, current FCC regulations permit high-rate (above 110MB/s) data transmissions over a short range (10-15m) at very low power. Major efforts are currently under way by the IEEE 802.15 Working Group for standardizing UWB wireless radios for indoor multimedia transmissions.

The targeted applications for UWB technology are those that traditionally suffer from a multipath fading effect that hamper indoor high-speed communications and positioning, ground penetrating radars, through-wall and medical imaging systems, and security systems.

2.3 SYSTEM CONSIDERATION FOR UWB IMPLEMENTATION

Traditional UWB systems rely on ultra-short waveforms that can be free of sine-wave carriers and do not require IF processing because they can operate at base-band. Because information-bearing pulses with ultra-short duration have UWB spectral occupancy, UWB radios come with a unique advantage that has long been appreciated by

the radar and communications communities. The main advantages of the UWB system are enhanced capability to penetrate obstacles, ultra high precision ranging at the centimeter level, a potential for very high data rates along with a commensurate increase in user capacity, all available in a potentially small size and processing power. Despite these attractive features, before 2001 interest in UWB devices was primarily limited to radar systems, mainly for military applications.

Currently there are two approaches for implementing UWB systems to use the FCC-allowed UWB bands, namely a pulse-based system and a carrier-based system.

Following the traditional approach to use wide bandwidth, a pulse-based system uses a modulated pulse to transfer information; this has been the method used in conventional military applications and in impulse radios. Because of the characteristics of the pulse, the RF front-end of such systems tends to be simple, with this simplicity serving to eliminate the need for the up-conversion or down-conversion that was required for traditional narrow-band systems.

In contrast, the carrier-based system is a version of the traditional narrow-band system that has been extended to accommodate a wide bandwidth. Therefore, its RF front-end architecture closely resembles that found in conventional narrowband systems.

2.3.1 DS-CDMA system

A DS-CDMA system follows the traditional approach to accommodate a wide bandwidth. An information-bearing signal is generated using very short, low-duty cycle and base-band electrical impulses [12]. Because no carrier is used to up-convert or down-convert the signal, such systems are often called carrier-free, base-band or impulse radio communication systems.

A single pulse with a certain repetition rate can show a peak in the frequency domain that can interfere with other existing communication signals. To alleviate this issue, the system incorporated a technique called the direct sequence spread spectrum (DSSS). By applying the DSSS technique, the energy contained in repeated pulses is spread over a wide frequency range, which alleviates the peaking problem caused by the single pulse approach. Since the system uses code division multiple access (CDMA), the system is called UWB direct sequence code division multiple access (DS-CDMA). Because of the difficulty of controlling the exact shape of the impulse, and consequently the overall frequency response, such systems tend to use the overall frequency band, and are sometimes also called single-band systems.

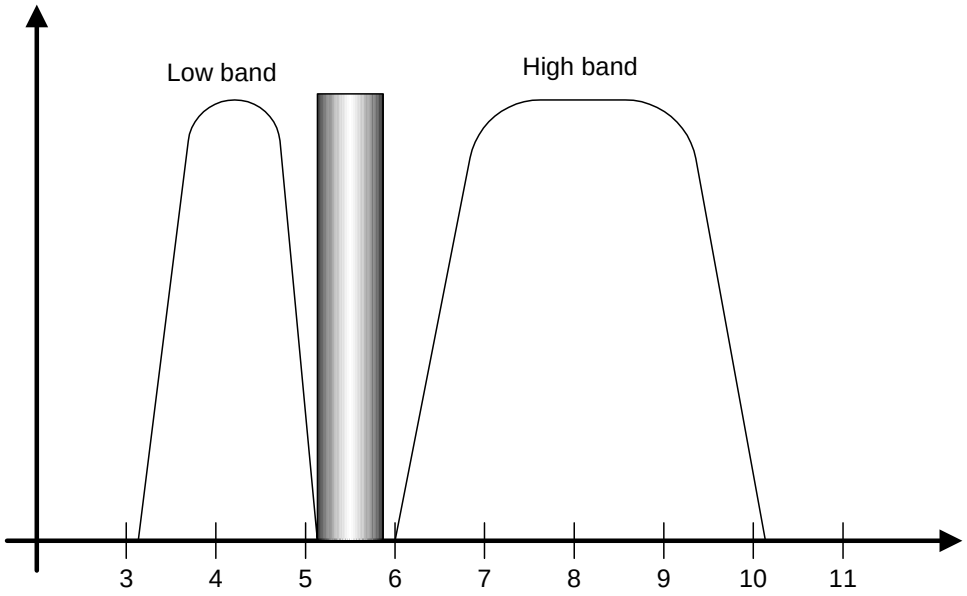


Figure 2.3 Spectrum usage of UWB DS-CDMA system

The DS-CDMA system uses a two-band approach as shown in Figure 2.3. The low band consists of the frequency spectrum from 3.1GHz to 5.15GHz, and the high band

spans from 5.825GHz to 10.6GHz. Since the UWB frequency spectrum overlaps the existing 802.11a system from 5.15 to 5.825GHz, this system avoids the use of the overlapping frequency ranges.

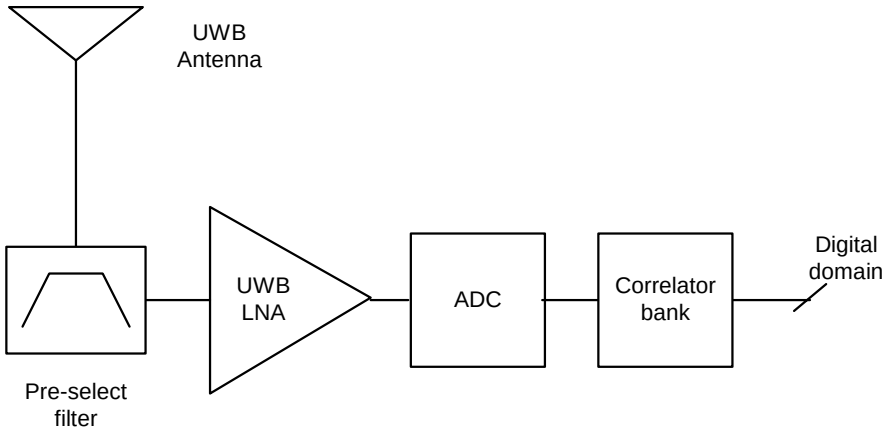


Figure 2.4 Simplified RF receiver architecture for a UWB DS-CDMA system

Figure 2.4 shows a potential architecture for the UWB DS-CDMA system. The RF portion of the system requires an ultra-wideband antenna, a bandpass filter to filter out the out-of-band interferers, and an LNA. The correlator bank can be implemented using analog circuits and depending on the sampling rate of the ADC, can be placed before the ADC or in the digital circuits after the ADC.

2.3.2 MB-OFDM system

Another approach is to use the conventional wireless architecture to implement the UWB system [13]. This approach can be viewed as an extended version of

802.11a wireless LAN despite some differences, such as frequency hopping. In this system, the entire UWB spectrum is divided into several bands with a fixed bandwidth of 528MHz. Information is transmitted using orthogonal frequency division multiplexing (OFDM) modulation on each band. Since it uses several sliced bands with OFDM modulation, it is called a multiband OFDM (MB-OFDM) system. Since the system uses a carrier to transmit information, the system can be categorized as a carrier-based system, which is clearly different from the pulse-based DS-CDMA system. The details of the band plan are shown in Figure 2.5. Such a technique possesses better spectral control properties.

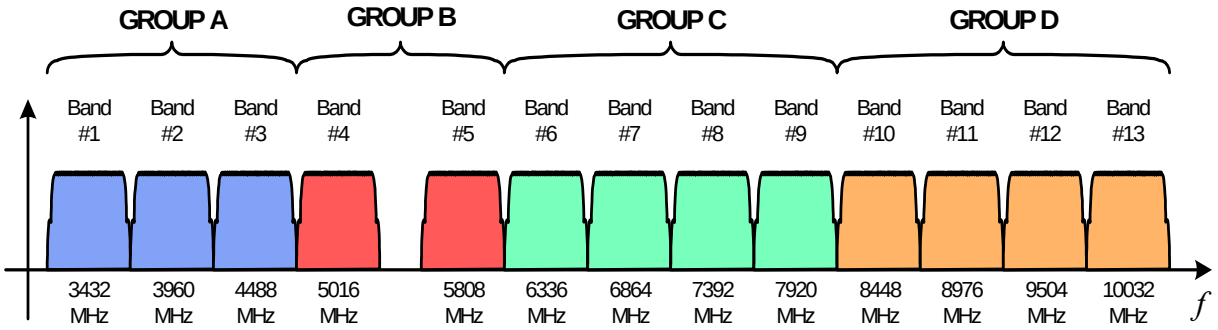


Figure 2.5 Band plan of the MB-OFDM system

OFDM allows good performance in a multipath environment and good immunity to narrowband interference. OFDM is spectrally efficient and allows shaping of the spectrum to avoid introducing any interference by eliminating specific carriers. However, OFDM is sensitive to phase noise, which introduces inter-carrier interference (ICI), and has a high peak-to-average power ratio (PAPR) that necessitates a large dynamic range in

signal processing circuits.

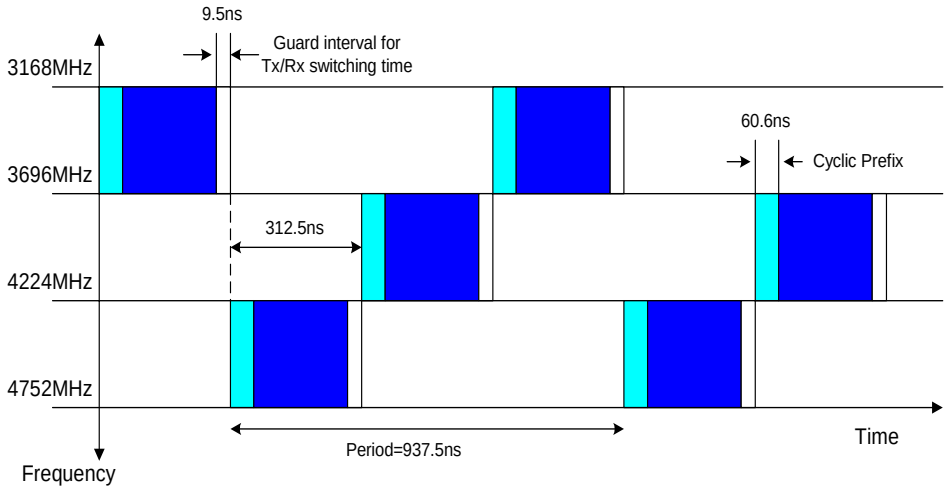


Figure 2.6 Example of time-frequency interleaving for the MB-OFDM system ("interleaving" OR "interweaving"?)

Figure 2.6 provides an example of how OFDM symbols are transmitted in a multiband OFDM system. This figure shows that the first OFDM symbol is transmitted on channel number 1, the second OFDM symbol is transmitted on channel number 3, the third OFDM symbol is transmitted on channel number 2, the fourth OFDM symbol is transmitted on channel number 1, and so on [14]. The use of frequency hopping with a short time interval introduces other design challenges. Figure 2.7 shows a simplified RF front-end architecture for the MB-OFDM system. The RF architecture seems similar to the conventional direct conversion scheme used for a narrowband application. However, the architecture should cover all the UWB frequency bands, which span from 3.1GHz to 10.6GHz. Covering this tremendous spectrum with an architecture that has been mainly used for narrowband applications is a great challenge in RF front-end implementation.

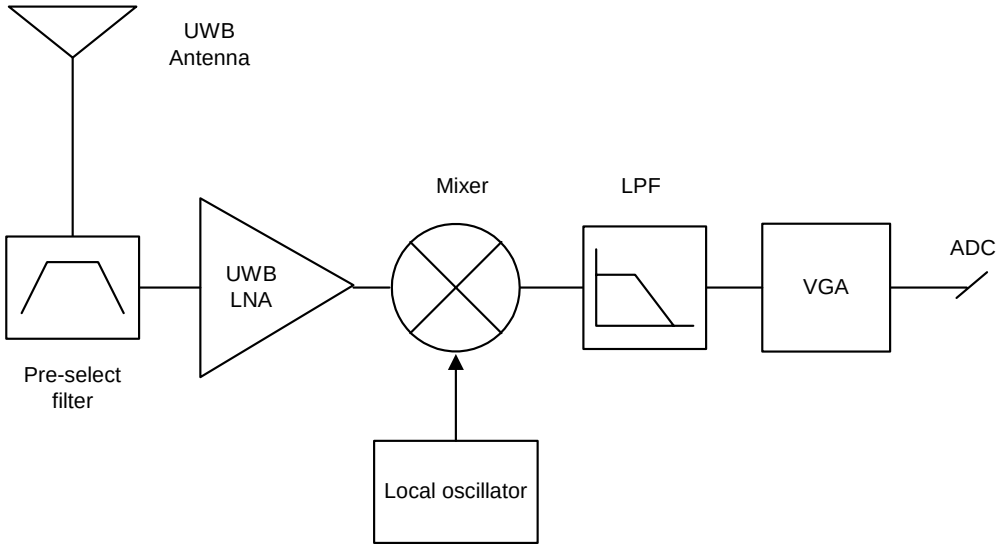


Figure 2.7 Simplified RF receiver architecture for a UWB MB-OFDM system

2.4 CHALLENGES IN RF FRONT-END IMPLEMENTATION FOR BOTH SYSTEMS

A lot of debate is under way about which system is more appropriate for implementing the FCC-allowed UWB system. The debate involves numerous issues, such as power emission, implementation complexity caused by the modulation incorporated, achievable data rate, multiuser capability, and so on. At a glance, the DS-CDMA system uses a simpler RF front-end than the MB-OFDM system. This is misleading, however, because in comparing the two systems, not only is the RF architecture different, but also the design considerations for each block (for example, the LNA) are different as well. These differences arise from the different frequency planning and system characteristics.

The DS-CDMA system utilizes two bands to convey information. Each band occupies the spectrum of 2GHz and 4GHz, respectively. The large spectrum of each band must be processed using an analog-digital-converter (ADC) to be handled in the digital

domain. Typically, the total power consumption of the ADC is proportional to the operating bandwidth that an ADC can cover [15]. Processing this extremely wideband signal using an ADC would be quite challenging and also would lead to high power consumption. The system requires over 20dB of gain and a less than 6.6dB noise figure (NF) in the RF front-end. Since the LNA is the only active RF component in the system, the LNA should have a gain higher than 20dB with a NF of less than 6.6dB while consuming a reasonable amount of DC power. Furthermore, the LNA needs to maintain the gain and NF over a very wide bandwidth of between 3.1 and 10.6GHz for a full-band UWB receiver. Input matching of the LNA cannot be ignored because it affects the overall system implementation margin, thereby requiring a good input matching of the LNA over the UWB frequency range.

Because the DS-CDMA system incorporates a wideband signal, it gives rise to a unique problem that had negligible impact on narrowband circuit designs. A flat group delay should be maintained for the whole signal bandwidth. A small group delay variation is desirable because this implies that all frequencies will be delayed relatively the same amount while passing through the amplifier. If all the various frequencies are not delayed equally, dispersion occurs and the output does not retain its identity [16].

The MB-OFDM system divides the entire FCC-allowed UWB spectrum into several 528MHz bands. The system also requires mixers and local oscillators to down-convert the RF signal into the base-band signal. Since digital information is transmitted using OFDM modulation, the system requires a Fast Fourier Transform (FFT) for a receiver and an Inverse Fast Fourier Transform (IFFT) for a transmitter, which increases the complexity of the system implementation.

Since the system uses a bandwidth of just 528MHz that is relatively small compared to the over 2GHz signal bandwidth in the DS-CDMA system, the group delay variation requirement in the RF front-end and the design of the ADC can be relaxed. The required gain of over 20dB in the RF front-end can be distributed between the LNA and the mixer, thus loosening up the design specifications of the LNA. However, the RF front-end needs to have a good input matching, and sustain reasonably constant gain and a noise figure of less than 6.6dB over the UWB frequency range. One of the challenges in implementing the RF front-end direct-conversion receiver for the UWB MB-OFDM system is that its local oscillation (LO) signal must cover the entire UWB frequency bands. The fundamental oscillation frequency tuning range is determined by the tenability of the LC resonator. Thus, it is highly unlikely that a single oscillator can cover the whole UWB frequency range. Furthermore, because of the frequency hopping nature of the MB-OFDM system, band-switching should be done within a guard interval of 9.5ns, which aggravates the design of the LO frequency synthesizer.

CHAPTER III

DESIGN OF ULTRA-WIDEBAND LNA

3.1 PREVIOUS APPROACHES IN THE DESIGN OF WIDEBAND LNA

Several different approaches have been proposed to establish a universal standard for such UWB applications [12,13]. Whether it is the pulse-based DS-CDMA system or multiband OFDM (MB-OFDM) system, the basic requirement of the UWB transceiver is a wideband low noise amplifier (LNA). The LNA needs to cover a wide range of frequencies from 3.1GHz to 10.6GHz, along with exhibiting low noise figure and low power consumption.

Traditional narrowband LNA designs use the cascode topology along with inductor degeneration to achieve good linearity and noise matching. However, this topology is based on the cancellation of the reactance for a narrow frequency range by using an inductor, and thus is not suitable for wideband operation.

Previously reported papers on the wideband LNA design utilized a Darlington pair [6][17], filters for a wideband input match [18,19], noise cancellation technique [20], and distributed amplifier [21]. Although these approaches can obtain the required gain over the wide frequency range, their high DC power consumption is unsatisfactory for most UWB applications.

In this chapter, a traditional resistive feedback topology is revisited for the UWB LNA design. Critical design factors such as the noise figure, group delay variation and linearity over the wide frequency range are analyzed. As a result, we demonstrate the design and implementation of a fully integrated UWB LNA with a low noise figure of less than

3.3dB and a low group delay variation of only 22ps from 2GHz to 10GHz, with power consumption as low as 9.6mW.

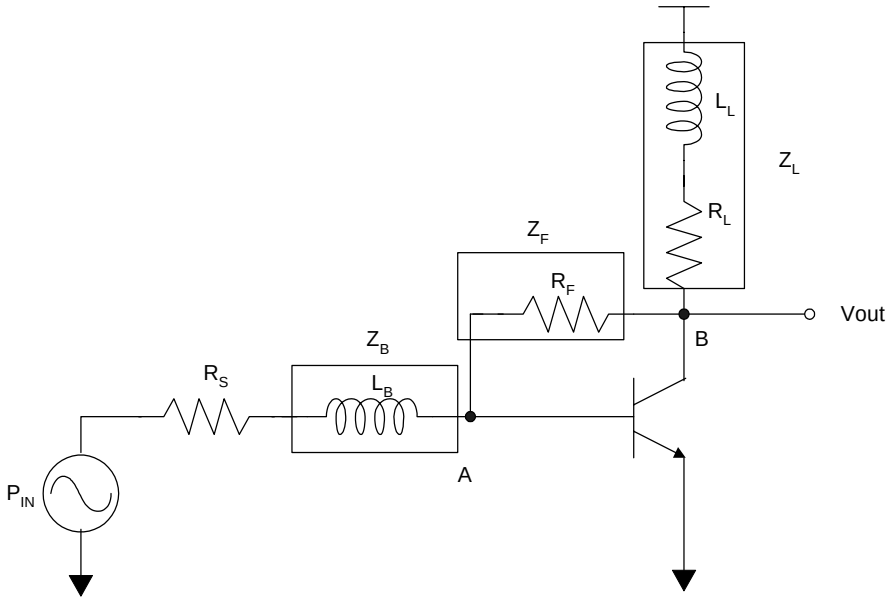


Figure 3.1 A resistive feedback low noise amplifier

3.2 DESIGN CONSIDERATION FOR UWB LNA

Several issues are encountered in designing a wideband low noise amplifier. The amplifier should minimize the input power loss, which is caused by a mismatch with the antenna. Maintaining a low noise figure over the wide bandwidth is another major concern. Wideband LNAs tend to have an extraordinarily high power dissipation compared with other LNAs of similar noise performance [17]-[21]. The high power consumption is due to its broadband characteristics, and hence techniques that reduce

power consumption through LC tuning are inapplicable [22]. Linearity cannot be ignored in the design, although its specification is rather relaxed compared with that of conventional narrowband LNA applications. Because the frequency component of the transmitted signal should experience the same delay amount to be properly recovered, the group delay variation in the RF front-end should be minimized.

3.2.1 Input match

A resistive feedback low noise amplifier is shown in Figure 3.1. For a UWB system, the input loss should be minimized over a wide bandwidth. A resistive feedback can have a reasonably good input power match because its input impedance is mainly set by frequency invariant terms, as given in Eqn.3.1.

$$Z_{IN} = Z_B + \left(r_\pi // \frac{Z_F}{1 + g_m Z_L} \right) \qquad (3.1)$$

The small-signal transconductance, g_m, is a frequency invariant term. Thus, the overall input impedance is set by the $Z_F/(1+g_mZ_L)$ term. As Z_F is usually a resistor, the input matching for maximum power transfer can be achieved over a wide frequency range. However, the feedback resistance Z_F controls input impedance as well as noise performance and a 3dB bandwidth, thus requiring careful optimization of its value to achieve low noise performance with a wideband operating frequency range.

3.2.2 Noise figure

The UWB specification requires the RF front-end to cover frequencies from 3GHz to

10GHz with a low noise figure and high gain for low DC power dissipation. Even though resistive feedback is generally known for its degradation in gain and noise performance in a trade-off of the extended operating bandwidth, further analysis is required to facilitate optimal design.

$$F = F_{\min} + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right] \quad (3.2)$$

The noise factor can be expressed in terms of F_{min} and the source admittance [23]. The noise performance of an amplifier is determined mainly by its minimum noise factor and noise contribution that occurs when input source admittance is different from its optimum admittance. Because of the wideband input matching characteristics of a resistive feedback, noise contribution from the second term in Eqn.3.2 can be minimized compared with F_{min}, and low noise performance over a wide bandwidth can be achieved by minimizing F_{min} .

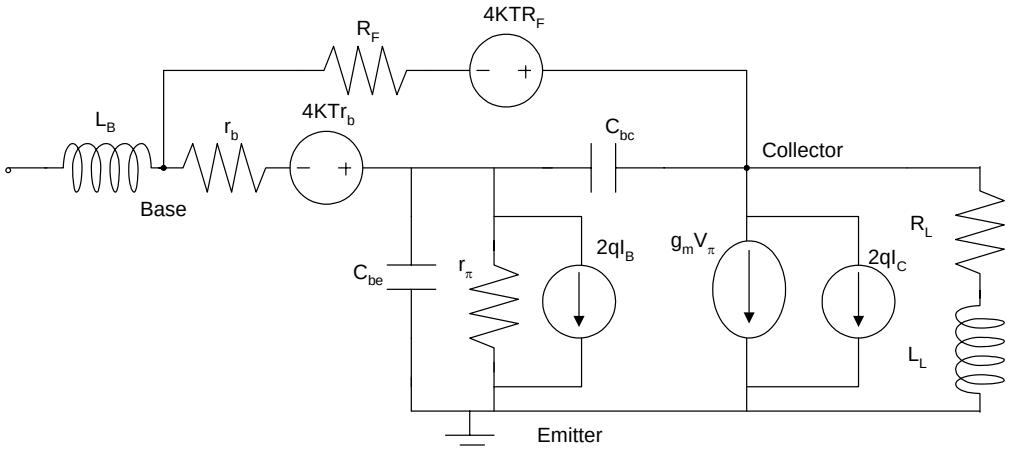


Figure 3.2 Small signal noise model of a resistive feedback SiGe HBT amplifier

The small signal noise model of the resistive feedback SiGe amplifier is shown in Figure 3.2, where r_b is the base resistance due to the current crowding effect, C_{be} is base-emitter junction capacitance and diffusion capacitance, C_{bc} is base-collector junction capacitance, and, Z_L and R_F are, respectively, load and feedback impedances.

The primary RF noise sources in a bipolar transistor are the base current shot noise $2qI_b$, the collector current shot noise $2qI_c$, the base resistance-induced thermal noise $4kTr_b$, and the feedback resistance-induced thermal noise $4kTR_F$. From the small signal noise model of Figure 3.2, an expression for minimum *NF* can be derived as in Eqn.3.3. A more detailed derivation for noise is illustrated in Appendix A.

$$NF_{\min} \cong 1 + \frac{g_m}{g_o^2}\left(g_f + \frac{g_m}{\beta}\right) + \frac{g_m^2}{g_o^2}\sqrt{2g_m r_b}\sqrt{\frac{1}{g_m^2}\left(\frac{g_o^2}{\beta} + g_f^2\right) + \left(\frac{f}{f_T}\right)^2} \quad (3.3)$$

where $g_f = \frac{1}{R_F}$ and $g_o = g_m - g_f$ (3.4)

From Eqn.3.3, we can see that the minimum *NF* increases with collector current through the g_m term. In addition, a reduction in base-emitter capacitance and in base-collector capacitance improves the minimum *NF* because the reduction in both capacitances increases the f_T of the device. By increasing current gain β, minimum *NF* can be reduced as well. The base resistance r_b typically plays an important role in determining the noise figure of conventional low noise amplifier design. Choosing a proper device geometry can strongly affect the design of wideband LNA. Overall, the

minimum *NF* decreases as the value of the feedback resistor increases, which is related to the operating bandwidth in this design. Thus there is an inherent trade-off in the operating bandwidth and noise performance in wideband resistive feedback LNA design.

The minimum *NF* increases as the frequency increases. In Eqn.3.3, the two terms inside the second square root become equal at a specific frequency, which defines a transition of the minimum *NF* from a white noise behavior to a 10dB/decade increase as the frequency increases. That transition frequency is defined in Eqn.3.5.

$$f = \frac{f_T}{g_m}\sqrt{\frac{g_o^2}{\beta} + g_f^2} \qquad (3.5)$$

As g_f increases, the frequency that defines a transition from white noise behavior to a 10dB/decade increase of minimum *NF* also increases. Suppose, for instance, that f_T is 100GHz and β is 200; then in this case the transition occurs around 7GHz without the resistive feedback from Eqn.3.5. The transition frequency can be increased as g_f increases. However, a reasonable transition frequency is around 10GHz for our purpose in considering operating bandwidth and noise performance for a given bias condition.

As derived in Appendix A, the expression of optimum source susceptance for the low noise matching is shown in Eqn.3.6.

$$B_{s.opt} = -\frac{g_m \omega C_i}{2 g_o R_n} \qquad (3.6)$$

$$X_{s.opt} = \frac{-B_{s.opt}}{G_{s.opt}^2 + B_{s.opt}^2} = \frac{\omega C_i}{K + (\omega C_i)^2} \qquad (3.7)$$

where $K = \frac{g_o^2}{\beta} + (1 + \frac{2}{\beta}) g_F^2$ (3.8)

Therefore, the required inductance L_B for low noise matching is

$$L_B = \frac{1}{\omega^2 C_i + \frac{K}{C_i}} \qquad (3.9)$$

A resistive feedback reduces the optimum source susceptance, $B_{s.opt}$, thus increasing the required input inductance for noise matching compared with the case without the feedback or the case with inductor degeneration. The latter is predominatly used in the conventional narrowband LNA design.

One advantage of noise matching at high frequency is that it can reduce the required input inductance. By matching noise at the high-end frequency, this small increase in inductance can be compensated for, and the required input inductance can be reduced. As a result, overall noise performance can be improved because a high quality inductor can be used. Therefore input noise matching at the high-end frequency will ensure the low noise performance of the amplifier over a wide bandwidth.

3.3 GROUP DELAY VARIATION ANALYSIS

A small group delay variation is desirable because this implies that all frequencies will be delayed relatively the same amount while passing through the amplifier. If the various frequencies are not delayed equally, dispersion results and the output does not retain its identity [16]. These effects are severe in the case of applied pulsed input signals, which

have distributed power over a wide bandwidth.

Group delay variations are considered in high speed wireline equalizer design, which also are required to operate over a wide bandwidth. However, the design consideration between the high speed equalizer and the UWB applications is quite different because the former contains the main signal energy around the DC region while the latter actually spread the signal energy over the entire band.

3.3.1 Group delay variation

Basically the group delay is a derivative of the phase of transfer function. For a transfer function *H(s)* with *s=jω,*

$$H(j\omega) = \left|H(j\omega)\right| \cdot e^{j\theta(\omega)} \qquad (3.10)$$

where $\left|H(j\omega)\right|$ and $\theta(\omega)$ are the gain and the phase components of the transfer function, respectively.

Phase delay and group delay are expressed as follows:

Phase delay $P_d(\omega) = -\dfrac{\theta(\omega)}{\omega}$ (3.11)

Group delay $G_d(\omega) = -\dfrac{\partial\theta(\omega)}{\partial\omega}$ (3.12)

Basically, the phase delay represents the absolute delay, and thus is of little significance. However, the group delay is used as the criterion to evaluate phase nonlinearity. Since the expression for group delay can be derived from the small signal transfer function, we will first consider the model shown in Figure 3.3.

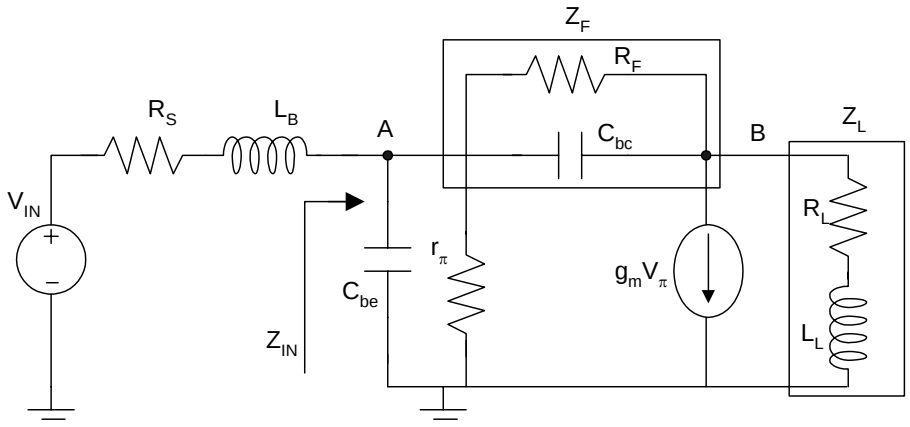


Figure 3.3 Small signal model of resistive feedback LNA for the analysis of group delay variation

$$A_V(s) = \frac{Z_{IN}}{R_S^{'} + Z_{IN}} \cdot \left(\frac{1 - g_m Z_F}{Z_F} \right) \cdot \left(Z_L \,//\, Z_F \right) \qquad (3.13)$$
$$= H_1(s) \cdot H_2(s)$$

where

$$Z_{IN} = \left(Z_L + Z_F \right) \cdot \frac{1}{1 + (Z_L + Z_F)\left(\frac{sC_{be}}{1 + sC_{be} r_\pi} \right) + g_m Z_L} \qquad (3.14)$$

$$R_S^{'} = R_S + sL_B \qquad (3.15)$$

The small signal gain A_v for the given circuit is expressed in Eqn.3.13. The equation can be divided into two parts. One is the voltage transfer function, $H_1(s)$ from input, V_{in} , to point A, and gain term, $H_2(s)$ from point A to point B. Intuitively, since group delay is the derivative of the phase of the transfer function, any resonance in the signal path will

contribute distortion in the group delay. The main contribution comes from the Miller effect. Because the input capacitance becomes large due to Miller effect, it can resonate with the input inductance. Since this resonance is in the direct path of the input signal, the critical part for group delay variation comes from $H_1(s)$, and the input can be approximated as in Figure 3.4.

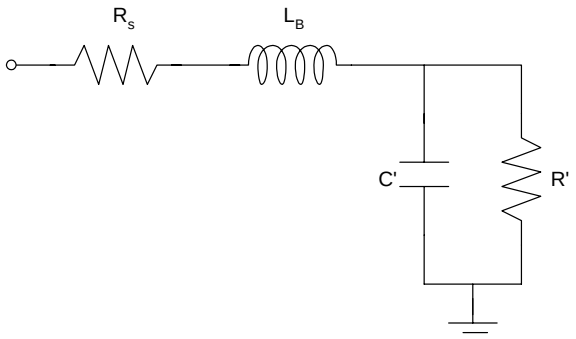


Figure 3.4. Simplification of input part of a resistive feedback amplifier.

$$H_1(s) = \frac{1}{s^2 L_B C' + s\left(\frac{L_B}{R'} + C' R_S\right) + 1 + \frac{R_S}{R'}} = \frac{1}{\frac{s^2}{\omega_o^2} + \frac{s}{\omega_o Q_o} + 1 + \frac{R_S}{R'}} \qquad (3.16)$$

where $$C' = \left| C_{be} + C_{bc}(1 + g_m Z_L) \right| \qquad (3.17)$$

$$R' = \frac{R_F}{1 + g_m Z_L} // r_\pi \qquad (3.18)$$

The transfer function of $H_1(s)$ can be approximated as in Eqn.3.16.

Suppose $R' >> R_s$, The equation is similar to that of second order low pass filter

transfer function, whose group delay variation depends on ω_o and Q_o [24]. The group delay of Eqn.3.16 is derived as in Eqn.3.19:

$$G_d(\omega) = \frac{1}{\omega_o Q_o}\left[\frac{1+\frac{R_S}{R'}+\left(\frac{\omega^2}{\omega_o^2}\right)}{\frac{\omega^4}{\omega_o^4}+\left(\frac{1}{2Q_o^2}-2\left(1+\frac{R_S}{R'}\right)\right)\frac{\omega^2}{\omega_o^2}+\left(1+\frac{R_S}{R'}\right)^2}\right] \qquad (3.19)$$

The equation indicates that at ω_o frequency, if Q_o is bigger than 0.577, the denominator of Eqn.3.19 has two poles in the imaginary part, which results in the group delay peaking [24]. Therefore group delay variation can be minimized either by increasing ω_o or by decreasing Q_o below 0.577.

From Eqn.3.16,

$$\omega_o = \frac{1}{\sqrt{L_B C'}} \qquad (3.20)$$

$$Q_o = \frac{\sqrt{L_B C'}}{\frac{L_B}{R'}+C' R_s} \qquad (3.21)$$

Since basically *R'* and *C'* are related to the amount of feedback, which is the main factor to determine the operating bandwidth, the best way to minimize the group delay variation is to reduce the value of L_B as much as possible, thus moving the ω_o term out of the required bandwidth. The effect is shown in Figure 3.5 through simulation. Figure 3.5 shows that the increases of L_B result in the increases of group delay variation because ω_o

falls into the operating bands. Therefore, the base inductance plays an important role in minimizing group delay variation.

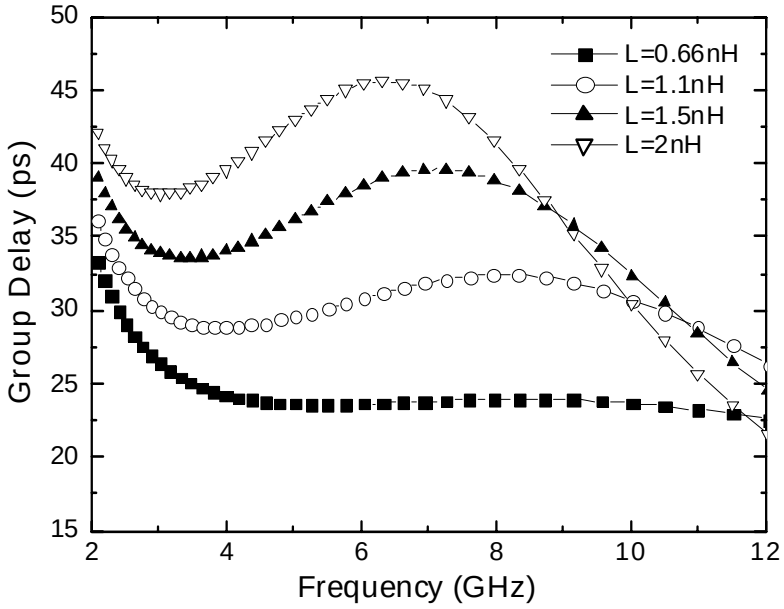


Figure 3.5 The effect of the input inductance on the group delay variation.

3.3.2 Optimum load impedance

For low power design, the device is mainly biased at its best noise performance. Therefore it might not achieve the required bandwidth or the gain flatness in the bandwidth. Inductive load is quite helpful, since it can boot up the gain as the frequency increases while the intrinsic gain of the device decreases as the frequency increases. The concern about load inductance is that it can distort the group delay variation as discussed in [25].

As can be seen in Eqn.3.20, the load impedance also affects the group delay variation by reducing ω_o. Therefore the maximum value of the load impedance that can minimize

the group delay variation exists.

In order to ensure the flat group delay variation, the following equation holds, where ω_o is high-end frequency, which is 10GHz in UWB applications.

$$\omega_o = \frac{1}{\sqrt{L_B C'}} \geq = \omega_{end} \qquad (3.22)$$

Since C' is related to the load inductance L_L as in Eqn.3.17, we can obtain the following expression by solving Eqn.3.22.

$$L_L \leq \sqrt{\frac{1}{\omega_o^2}\left(\frac{K}{C_i \cdot g_m^2 \cdot C_{be}^2 \cdot \omega_o^4} - R_L^2\right)} \approx \frac{R_L}{\omega_o} \qquad (3.23)$$

In the design, R_L is set mainly for linearity in the SiGe device considering its bias current. Once R_L is set, then the value of the load inductor can be determined using Eqn.3.23, which guarantees low group delay variation over the entire bandwidth.

The calculated value from Eqn.3.23 can be used as an initial value for the design. Since the delay variation not only depends on ω_o but also on Q_o, the calculated value for load inductance can be increased as long as Q_o is less than 0.577.

3.4 LINEARITY ANALYSIS

Linearity behavior in the wideband is different from conventional narrowband circuit design. In narrowband applications, the receiving bands are usually selected by a

preselect filter, eliminating high interferers from other applications. Therefore, their linearity considers only their input 1dB compression point (P1dB) and input third order intercept point (IIP3), which cannot be removed by a preselect filter.

The challenge in the UWB system is that the frequency band allocated for the system overlaps with other existing applications that may be near the range of the UWB system. The major interference would come from 802.11a, for instance, because it and the UWB share frequency bands. Although its transmitted and received signal strength is very low compared with the conventional narrowband system, the linearity of the LNA cannot be ignored because there is virtually no control over the high interferers, such as from 802.11a, that might cause the RF front-end of the UWB system to saturate.

Generally, the linearity improves as current consumption increases. Because the power consumption of the LNA should be minimized in UWB applications, there is a motivation to analyze the design concerning its linearity performance while reducing its power consumption.

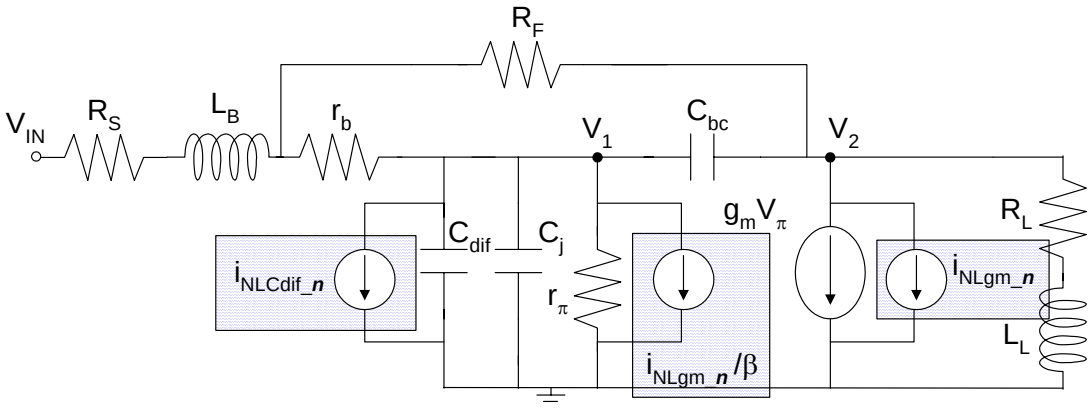


Figure 3.6 Nonlinear equivalent model of resistive feedback SiGe HBT LNA for low DC current

A Volterra series analysis was performed on the LNA to gain insight into its linearity behavior in a wide bandwidth. In this analysis, it is assumed that the input signal is very weak so that the I-V and C-V nonlinearities of an order higher than three are negligible, which is typical for LNAs because they operate far below their 1-dB compression point [26].

Figure 3.6 shows the nonlinear model of SiGe LNA used to derive the Volterra-series equation of a resistive feedback circuit in Figure 3.1. In this model, C_{dif} is the diffusion capacitance, which is proportional to the collector current and the forward transit time τ_F. C_j is the base-emitter junction capacitance. The main factors that affect the nonlinearity of the SiGe LNA under the low dc bias condition can be categorized into two, I-V nonlinearity and C-V nonlinearity [27]. In I-V nonlinearity, base current I_b and collector current I_c are controlled by the nonlinear function of the control voltage V_{be}. In C-V nonlinearity, C_{dif} is the strong function of V_{be} when the diffusion capacitance dominates because the diffusion charge is proportional to the I_c.

The nonlinear output current with the Volterra series when the input voltage V_{in} is applied is as follows [28],

$$I_c = G_1(s) \circ V_{in} + G_2(s_1, s_2) \circ V_{in}^2 + G_3(s_1, s_2, s_3) \circ V_{in}^3 + \cdots \quad (3.24)$$

Where V_{in} is the nth power of the voltage source signal and G_n is the Volterra series coefficient which is a linear function of n number of frequencies. The operator "o" indicates that each frequency component of V_{in} is changed by the magnitude and phase

of G_n [28].

The analysis is performed on the resistive feedback LNA as shown in Figure 3.1 with a device size of 0.2um × 15um, and the expression for third order intermodulation distortion (IMD_3) is derived as in Eqn.3.25. The details of the procedure to derive the Volterra series equation can be found in references [27]-[29].

As for its wideband linearity behavior, the expression of IMD_3 can be divided into three parts. *A* is related to overall linearity performance over the operating bandwidth; this performance can be improved mainly by consuming a large amount of current. *B* shows that IMD_3 can be reduced by canceling C_j with Z_g, which includes source impedance, R_s, and base inductance L_B. At low frequency, the cancellation effect is negligible. However the amount of cancellation increases as the frequency increases; therefore the IMD_3 performance generally improves with frequency. *B* and also suggests that the feedback resistance and load impedance should be as large as possible to minimize IMD_3.

$$
\begin{aligned}
IMD_3 &= \left|\frac{3G_3(s_a, s_a, -s_b)}{4G_1(2s_a - s_b)}\right| \\
&= \frac{V_T}{3}\left|\frac{G_1(s)}{I_C}\right|^3 && : A \\
&\times\left(1 + sC_jZ_g(s) + \frac{Z_g(s)}{Z_F(s) + Z_L(s)}\right) && : B \\
&\times\left[-1 + \frac{G_1(2s)}{2g_m}\left(1 + 2sC_jZ_g(2s) + \frac{Z_g(2s)}{Z_F(2s) + Z_L(2s)}\right)\right] && : C \quad (3.25)
\end{aligned}
$$

Because the load impedance is related to the group delay variation in this design, the value of the load inductor can be maximized as long as its degradation in group delay

variation is negligible.

C determines its wideband linearity behavior. It can be defined as a multiplication factor because its value, which is less than one, is multiplied to the previous *A* and *B*. While the IMD_3 improves along with frequency according to *A* and *B*, *C* suggests that there is peak degradation in linearity due to cancellation from its second harmonic terms. The effect is shown in Figure 3.7. Figure 3.7 shows the simulated IMD3 performance for the model shown in Figure 3.6 with a device size of 0.2um × 15um.

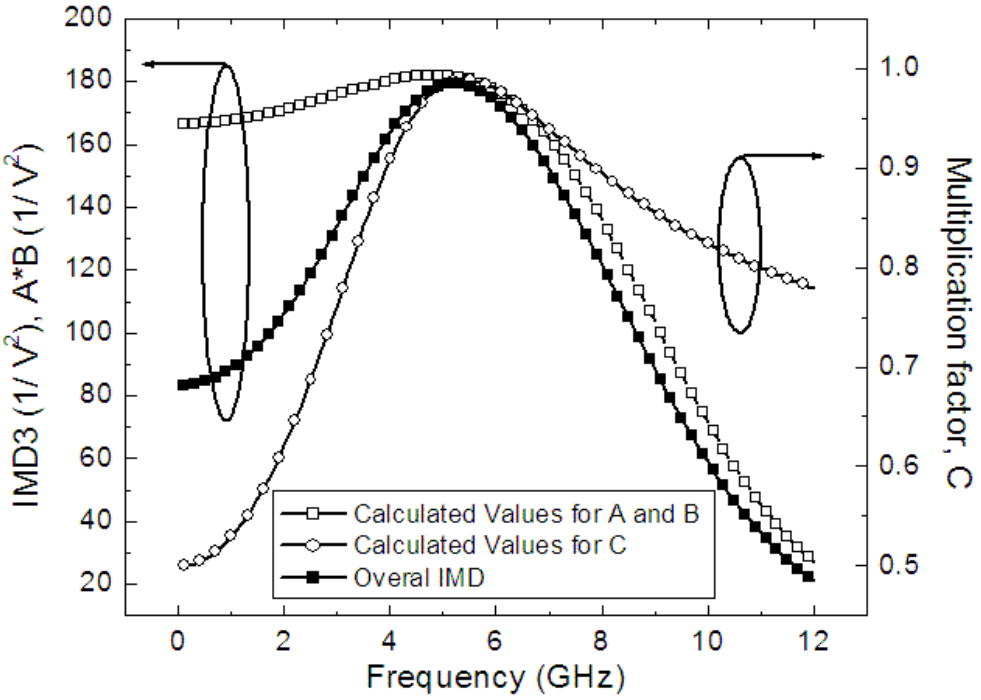


Figure 3.7 Simulated IMD3 performance from Volterra series analysis

Because the LNA has gain from 3GHz to 10GHz, the contribution from $G_1(2s)/2g_m$ in *C* differs between 3GHz to 5GHz and 5GHz to 10GHz. The first lower band benefits

from the cancellation in *C* while the higher band suffers from small cancellations caused by small $G_1(2s)/2g_m$ at high frequencies, which is contrary to the case in *B*.

Also the cancellation in $1+2sC_jZ_g(2s)$ cannot be ignored due to its high frequency term. In the design, $2sC_jZ_g(2s)$ cancels out '1', thus creating a peak degradation in the bandwidth. The frequency at which peak degradation in linearity occurs can be predicted by using the following equation.

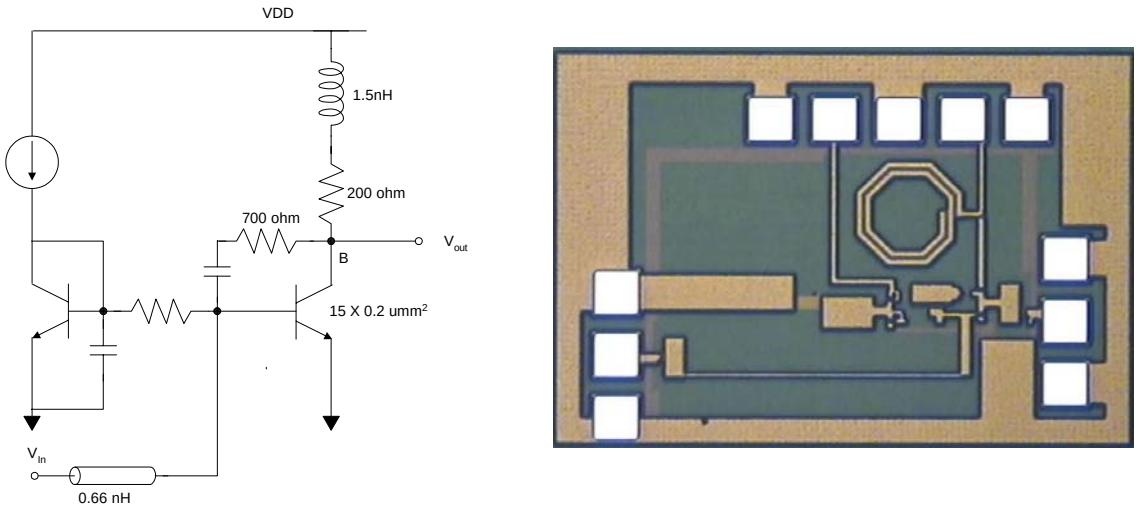
$$f_{IMD\_MAX} \cong \frac{1}{2\pi}\sqrt{\frac{1}{4L_BC_j}} \qquad (3.26)$$

Note that Eqn.3.26 shows that the frequency where the maximum degradation occurs in its linearity performance is related to the base inductance as well. Since base inductance is related to the noise and group delay performance of the LNA, the peak degradation in linearity cannot be avoided for UWB applications. However, by predicting its maximum degradation frequency in linearity, we might be able to move the frequency point to the unused frequency bands as discussed in [12,13]. This peak degradation must be considered in UWB LNA design, and the linearity specification must be satisfied.

3.5 CIRCUIT DESIGN OF UWB LNA

The base resistance, $r_{b,}$ is the main factor that increases the *NFmin* of the device, and it is related to the emitter width. The device with a smaller emitter width reduces *NFmin,* especially at high frequencies. The emitter length does not affect the achievable *NFmin*; however, it is related to the input matching and the linearity performance of the LNA. The minimum noise figure is proportional to frequency and the amount of feedback. A

SiGe HBT that has low C_i (=C_{be}+C_{bc}) and high f_T improves the gain and the *NFmin*.



(a) (b)

Figure 3.8 (a) Circuit schematic of the implemented UWB LNA on SiGe BiCMOS process (b) Chip photo of UWB LNA

The choice of feedback resistor, $R_{F,}$ determines the operating bandwidth and minimum noise figure of the amplifier. Low R_F increases the operating bandwidth with the sacrifice of the gain and noise performance. Consequently a R_F that is as high as possible and still remain within the bandwidth requirement should be chosen. To reduce DC power consumption and increase gain and noise performance, R_F is selected at a point at which it can barely meet the bandwidth requirement, and the rest of the bandwidth is covered by boosting its gain in high frequencies. By incorporating a load inductor, the flat gain over the wideband can be achieved. From the view point of gain flatness over the bandwidth, load inductance should be increased as long as it does not degrade the group delay variation.

Although a device with a small emitter width and a large emitter length can improve

the gain and noise performance, it lacks good linearity. The drawback in terms of linearity could be overcome by either increasing the DC bias current or by trading off the noise performance by using a rather large size of the device. Linearity can be improved by choosing a device with a large junction capacitance, which contributes to the cancellation of IMDs as seen in Eqn.3.25. Taking into considerations all these factors, the emitter width of 0.2um and length of 15um is chosen for the LNA device in Figure 3.8(a).

Noise matching is performed around 10GHz. A resistive feedback increases the value of the inductor for noise matching. By performing the noise matching at the high-end of the frequency band, not only the value of inductor decreases but also the noise figure within the operating bands decreases because the maximum noise figure would be at the high-end frequency.

Because the quality factor of the noise matching inductor affects overall noise performance, a transmission line inductor of 0.66nH with a Q of 20 is used in the implementation.

Load resistance R_L is selected to achieve a best IIP3 performance. V_{ce} performs an important role in determining the IP3 of the device itself. The value of R_L can be calculated using bias current and supply voltage to bias the device at its high tolerance point to the distortion. Once R_L is determined, the value of a load inductor that will have a minimal effect on the group delay variation is obtained.

3.6 MEASURED RESULTS

The designed UWB LNA is fabricated in IBM 0.18um SiGe BiCMOS process. The size of the fabricated IC is 1.1x0.8mm^2. The input and output ports are matched to the 50-ohm without using any buffer amplifier. The design is optimized to use the proper value

of passive devices considering their self-resonating frequencies (SRF) for operation up to 10GHz.

The measured and simulated S-parameters are plotted in Figure 3.9 and Figure 3.10. The measurements show a gain of 13dB with a 3dB bandwidth of 10GHz. Reverse isolation is better than 23dB over the entire band. An input return loss of -7dB at 3GHz is achieved, which improves up to -24dB at 10GHz for simultaneous noise and power matching. The measured output return loss is less than -10dB over the entire band.

The measured and simulated noise figures are shown in Figure 3.11. The noise figure of the LNA is between 2.9dB and 3.3dB from 2GHz to 10GHz. Uniform group delay variation of around 22ps is achieved for the entire UWB band, as shown in Figure 3.11.

Two tone measurements are performed at 3GHz, 5GHz, 7GHz and 10GHz with 200MHz spacing to measure the linearity of the amplifier over the entire band. The measured input compression point (ICP) and input third order intercept point (IIP3) at 3GHz are -14.5dBm and -6.5dBm, respectively.

The linearity is degraded around 7GHz as expected from Eqn.3.25 in the Volterraseries analysis. An IIP3 of -5dBm and input P1dB of -14dBm are measured at 10GHz.

The measured IIP3 and ICP performance of the LNA over the UWB frequency range is shown in Figure 3.12. Figure 3.13 shows that the measured IIP3 performance around 7GHz.

The fabricated UWB LNA consumes 4mA from a 2.4V power supply. When the current is reduced to 3mA, the 3dB bandwidth remains the same but the gain is reduced to 11.5dB with a 3.5dB NF at 10GHz. Since the design is optimized for low noise performance, the NF is not degraded much with a reduced gain. The designed LNA

achieves a low noise figure of 3.5dB while simultaneously consuming the least power (7.2mW) yet published in a commercial SiGe BiCMOS process.

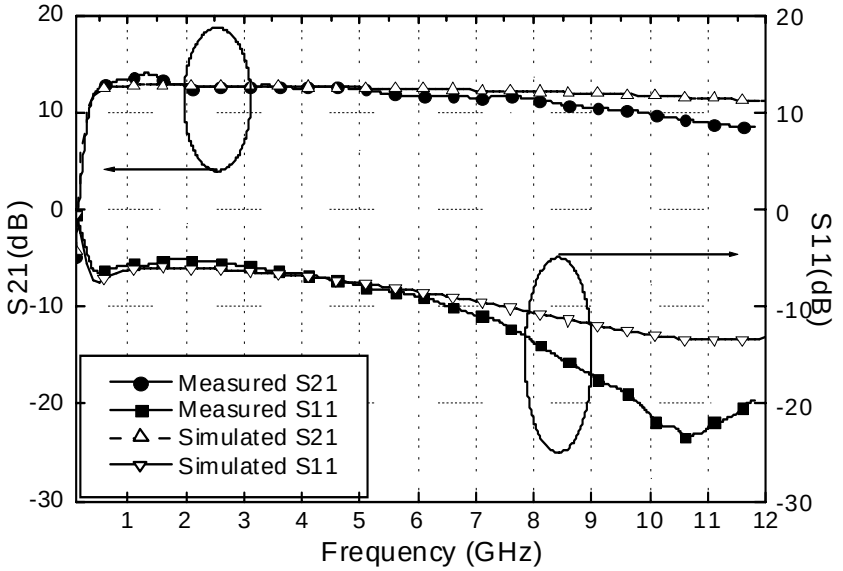


Figure 3.9 Measured and simulated S21 and S11 of the LNA

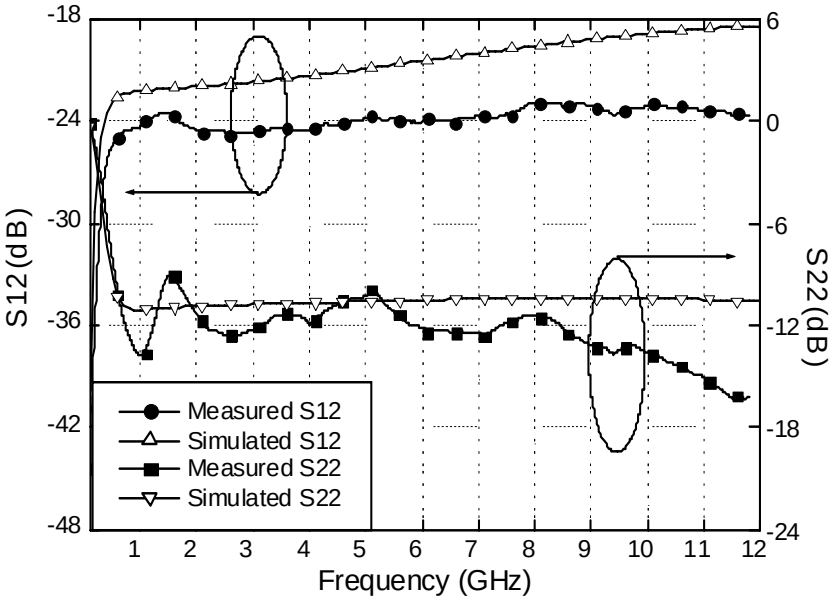


Figure 3.10 Measured and simulated S12 and S21 of the LNA

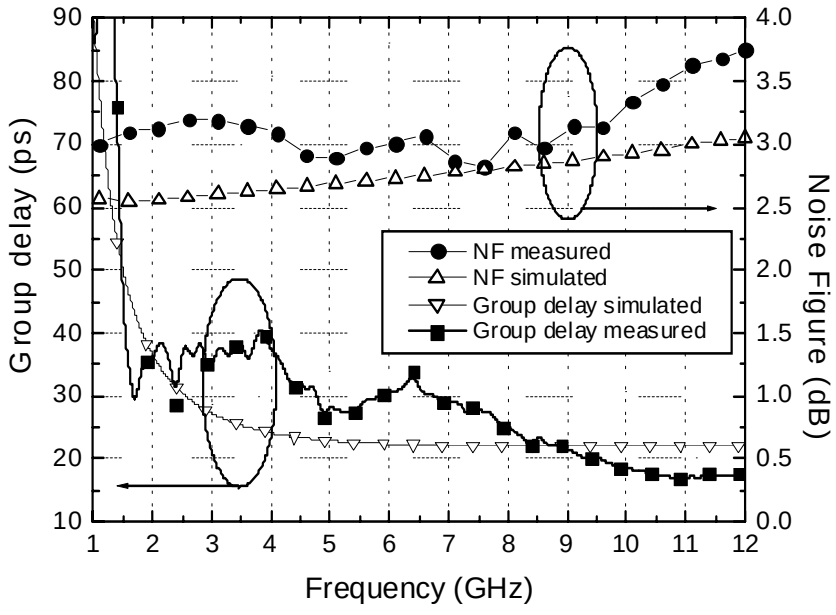


Figure 3.11 Measured and simulated noise figure and group delay of the LNA

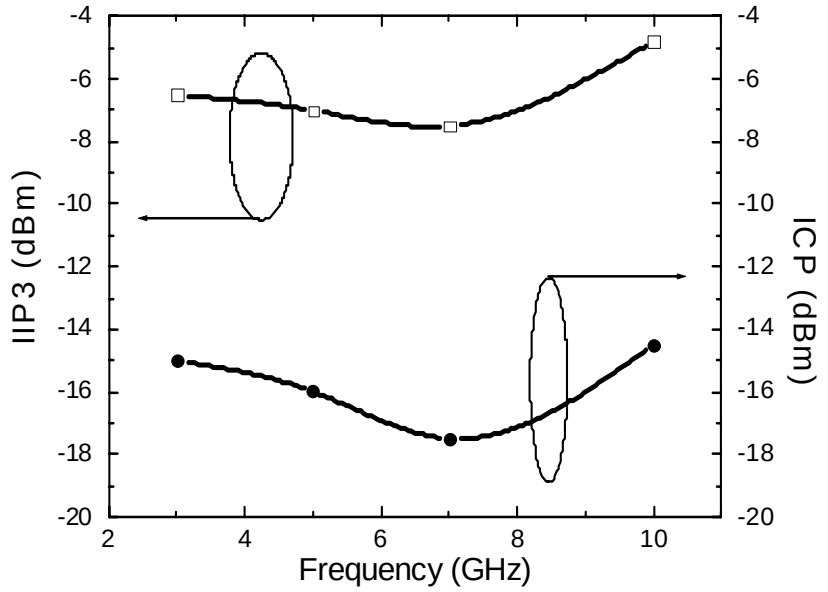


Figure 3.12 Measured IIP3 and ICP of the LNA over the frequency range.

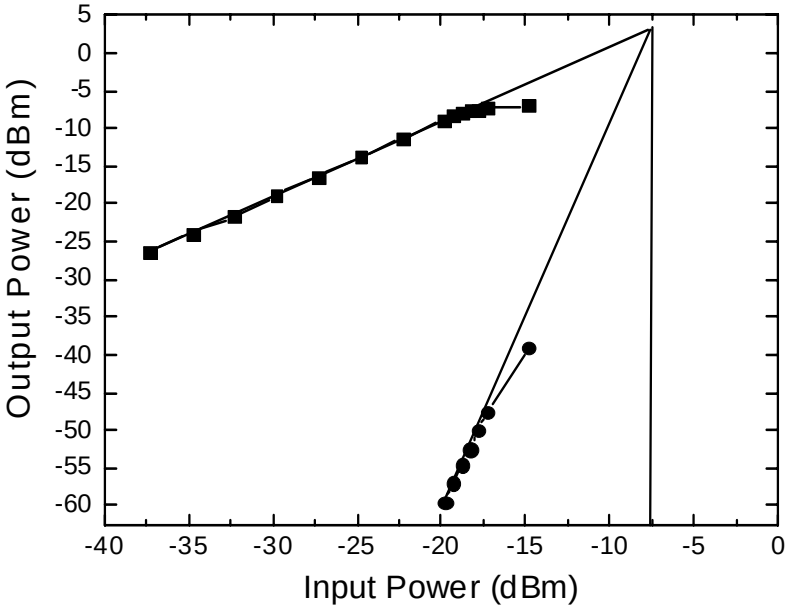


Figure 3.13 Measured IIP3 of the LNA at 7GHz

3.7 CONCLUSION

We have analyzed the key performance factors required for a UWB LNA design, such as noise performance, group delay variation, and linearity over a wide bandwidth. Through the analysis we determined that low base inductance was beneficial to achieve low group delay variation while maintaining low noise performance. A Volterra series was performed to obtain an insight into linearity behavior over the wide frequency range.

The fully integrated UWB LNA is implemented and fabricated in a commercial SiGe BiCMOS process. The design utilizes resistive feedback to achieve a flat gain and low noise figure over the entire band while consuming low DC power. The measured performance of the UWB LNA shows a low noise figure of 3.3dB, a low group delay variation of 22ps with compatible linearity performance over the entire UWB band while consuming total power as low as 9.6mW.

CHAPTER IV

IMPLEMENTATION OF UWB RECEIVER FOR MULTIBAND OFDM SYSTEM

4.1 MOTIVATION

As seen in Chapter 2, division of a large spectrum of 7.5GHz into several 528MHz pieces gives some advantages compared with the approach of using a whole frequency range from the perspective of the requirements for ADC and the group delay variation of passive components in RF front-end. These passive components include the UWB antenna and band-pass filter, which rejects out-of-band interferers. However, such relaxation in the requirement for ADC and group delay variation in some components can be obtained only at the sacrifice of more stringent performance requirement of the RF front-end. In Chapter 2, we briefly discussed a signal and modulation scheme for two different approaches to implement a UWB system: Those approaches were DS-CDMA and MB-OFDM systems. The DS-CDMA system, based on pulse approach, requires a LNA as the main RF circuit component. The MB-OFDM system, based on the carrier approach, requires an ultra-wideband LNA, and a mixer with a proper LO signal generation scheme, which needs to cover 3G-10GHz with mostly equal weightings.

In the MB-OFDM system, the LNA and mixer should be able to amplify the input signal with acceptable noise performance for a wide frequency range. The system has only a 3dB implementation margin in its budget, thus good input matching over a wide bandwidth of 3-10GHz should be ensured to minimize loss in the front-end [13]. The dynamic range of the LNA and mixer should be large enough not to degrade the bit error

rate (BER), which is related to linearity performance.

For a simple and low cost solution, a direct conversion is the proper architecture to implement an MB-OFDM UWB system. Because the RF signal is down-converted to the baseband with a LO signal, the LO signal also needs to cover from 3GHz to 10GHz. However, generating a LO signal for such a wide frequency range is difficult. Even more challenging, band switching should be done within a guard interval of 9.5ns, thereby aggravating the design of PLL.

One of the major challenges for the implementation of a RF front-end for an MB-OFDM system is that all the requirements listed above should be met with minimum power consumption, which is contrary to the generally accepted knowledge that wideband operating circuits tend to consume more DC power than narrowband circuits [6,30]. In this chapter, we will first discuss why a direct conversion is the proper approach for the implementation of the MB-OFDM UWB system. Then, the design of a mixer is investigated for its noise, linearity and conversion gain. Finally, the design and measurement of the receiver is demonstrated for a full-band UWB frequency range. The discussion of the RF implementation for the MB-OFDM UWB system is limited to the design of the receiver, excluding the LO signal generation scheme.

4.2 DESIGN CONSIDERATIONS FOR A UWB RECEIVER IMPLEMENTATION

The implementation of UWB receivers tends to rely on direct conversion because of its simplicity, low power consumption, and small size with a reduced components count. Traditionally, a direct conversion scheme suffers from several drawbacks that are not easily overcome in conventional narrowband systems such as GSM. These challenges include DC-offset generation, input IP2, flicker noise, LO leakage and radiation, and

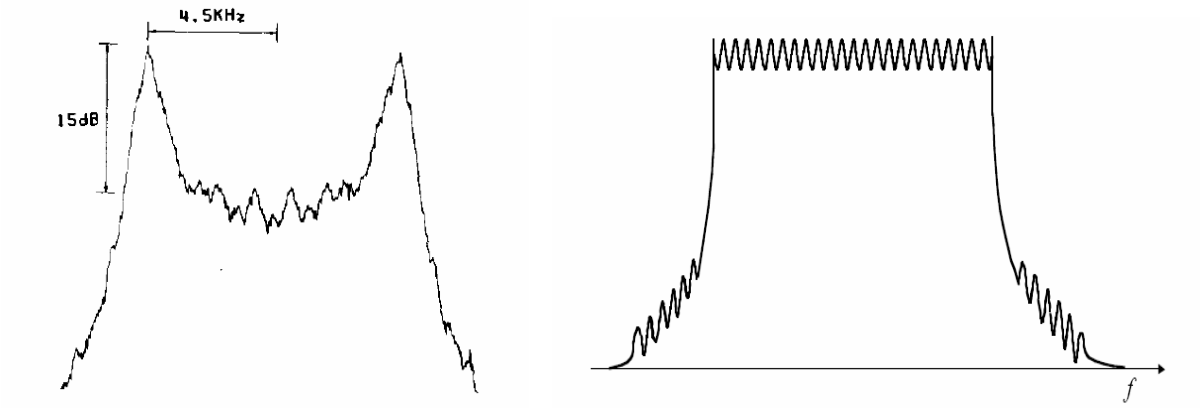
accurate I/Q signal generation. Since the UWB system utilizes a very wide bandwidth, some of the problems in a conventional direct conversion receiver may not be a problem in this case. On the other hand, designing a conventional direct conversion receiver for wide bandwidth may give rise to new problems.

4.2.1 DC-offset

One of the major challenges in implementing direct conversion is the degradation of signal to noise ratio (SNR) because of the presence of DC-offset and flicker noise. In traditional design of a direct conversion receiver, DC-offset generated in the receiver has been the biggest problem that had to be solved. Because a small DC-offset can saturate IF gain stages and the following stages as well because of high gain in the IF amplifier, several solutions to remove or reduce DC-offset have been devised. In the systematic approaches, DC-offset can be reduced through AC-coupling [31], using a servo amplifier [32] or digital signal processing (DSP) to cancel the offset; different LO frequency design has also been used [33]. From the aspect of circuit design, DC-offset is generated because of a mismatch in differential circuits. Therefore, proper layout technique that reduces mismatches also reduces DC-offsets.

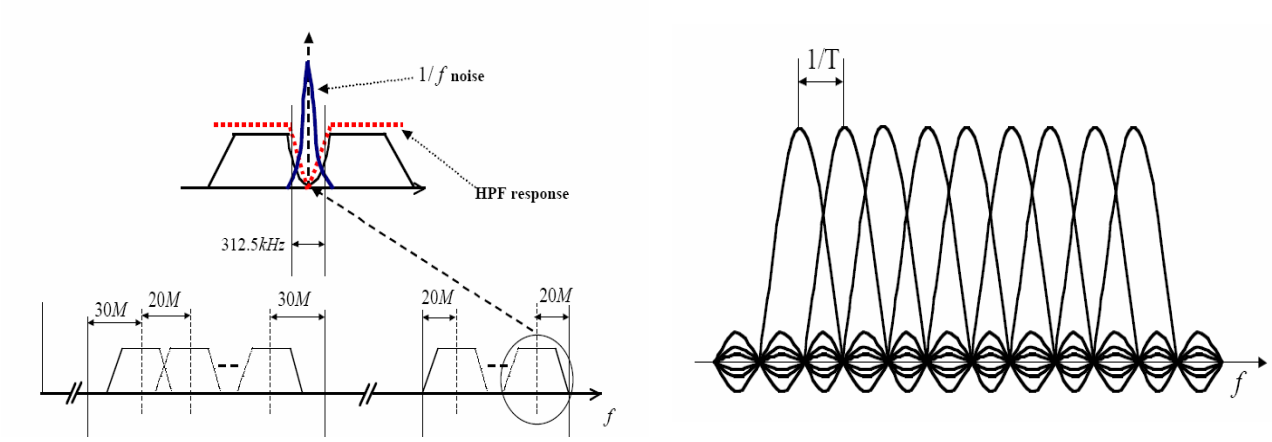
Also a proper modulation scheme with an AC-coupling technique can easily alleviate the DC-offset problem. Such a modulation scheme is called "DC-free modulation." This is usually done by not transmitting any data near the DC. One of the examples of "DC-free modulation" is orthogonal frequency division multiplexing (OFDM). Since OFDM can selectively remove its subcarrier, this modulation scheme is a proper candidate from a perspective of direct conversion implementation [34]. Another usable modulation scheme is FSK modulation in [31] because most of the signal energy

is concentrated on the FSK tone frequencies and little at the center.



(a) (b)

Figure 4.1 Spectrum of (a) FSK modulated signal and (b) OFDM modulated signal



(a) (b)

Figure 4.2 (a) Example of a DC-free modulation scheme (OFDM) by removing subcarrier of a OFDM signal (b) Spectral overlap of subcarriers in OFDM

4.2.2 Flicker noise

Since the down-converted spectrum extends to zero frequency, the flicker noise of

devices substantially corrupts the signal, which is a severe problem in MOS implementations. For this reason, it is desirable to achieve a relatively high gain in the RF range, for example, through the use of active mixers rather than passive mixers. In this regard, BJT and SiGe HBT have been known for their low flicker corner frequency. While CMOS has non-uniform channel trapping electrons when they are moving from source to drain, BJT and SiGe have a relatively uniform junction that results in low flicker corner frequency.

4.2.3 LO leakage and I/Q imbalance

Without proper isolation between a LO signal port and an antenna, the LO signal leaks to the antenna and radiates, creating interferers in the band of other receivers. Since the UWB system overlaps with existing communication systems, there is a limit on the power emission from the UWB system. The restriction on the emission is -41.3dBm/MHz. Even though this restriction is mainly applied to the transmitting power of the system, it also can be applied to the LO leakage and radiation.

When phase and frequency modulation schemes are involved, a direct conversion receiver must incorporate quadrature mixing. This requires shifting either the RF signal or the LO output by 90 degrees. As the mismatch in the I-channel and the Q-channel increases, the degradation in BER increases. This becomes severe when a dense constellation such as 16-QAM or 64-QAM is used as a modulation. For a fixed available bandwidth, incorporating a dense constellation modulation can increase the data rate. For example, Table 4.1 shows I/Q imbalance requirements for various modulation schemes in 802.11a. When a low data rate is involved, a more relaxed I/Q imbalance is required. However, a high data rate can only be achieved with more stringent requirements for I/Q

imbalance. Therefore, minimization of the I/Q imbalance in the receiver has usually been a challenge when a dense constellation modulation is used.

Table 4.1 I/Q imbalance requirements for various modulation schemes in 802.11a.

Data rate (Mbps)	Modulation scheme	Constellation error (dB)	Gain imbalance as phase imbalance=0	Phase imbalance as gain imbalance=0
12	QPSK	-10	1.9	25.62
18	QPSK	-13	1.36	18.14
24	16-QAM	-16	0.97	12.84
36	16-QAM	-19	0.69	9.09
48	64-QAM	-22	0.49	6.43
54	64-QAM	-25	0.34	4.56

The modulation scheme for the MB-OFDM system is limited to QPSK [13]. This is mainly because of a wide bandwidth available for the data transmission, which can achieve a target data rate of 110Mb/s at 10m distance without using a dense constellation modulation. Therefore, an allowable I/Q imbalance required for QPSK is less strict than in the case of 16 or 64-QAM. Nevertheless, a minimum I/Q imbalance should be maintained over a very wide bandwidth of 3-10GHz, a requirement that presents a new challenge in UWB receiver design. The phase noise specification for the system is relaxed because of the wide bandwidth of the utilized band.

4.2.4 Wideband input matching

Although the unique problems of implementing direct conversion architecture are taken care of relatively easily in a wideband system, there exist still some challenges. Since an MB-OFDM system achieves its target data rate (throughput) by maximizing the transmitted power levels within the restriction imposed by the FCC and by minimizing loss in the receiver, input loss should be reduced to a minimum to get satisfactory performance, which requires very good wideband input matching. In a conventional narrowband receiver, input matching was performed at the application frequency by matching it to 50 ohm. Since the frequency dependent elements such as the inductor and capacitor are usually used in matching, it is hard to achieve good input matching over a wide frequency range.

4.2.5 Wideband operation with low DC power consumption

As discussed in Chapter 3, noise, gain, and linearity are all correlated to the operating frequency range with a variable of power consumption. Wideband operating circuits tend to consume more power in order to achieve compatible performance in gain, noise, and linearity compared with narrowband circuits. Furthermore, traditional techniques using inductors and capacitors have been used in narrowband circuit designs to improve their gain, noise, and linearity while minimizing power consumption. Inductors and capacitors are intrinsically frequency-dependent elements, and their values are defined at one frequency. As a result, most of those techniques that were popularly used in the narrowband circuit designs are not applicable to wideband circuit designs. Therefore, achieving a low noise figure and enough gain with good linearity to support a BER of 10^{-3} can be challenges when the UWB devices are designed for power-hungry

handheld applications.

4.2.6 Noise figure and linearity of receiver

It is important to define the cascaded system parameters for direct conversion receiver implementation. The key parameters from the system perspective are gain, noise figure, and linearity.

According to Friis equation [35], the cascaded noise figure is computed by

$$F = F_1 + \frac{F_2 - 1}{A^2} \qquad (4.1)$$

Where F_1 is the noise figure (NF) of the LNA, F_2 is the NF of the mixer, and A is the loaded voltage gain from the LNA input to the mixer input. As seen in Eqn.4.1, the NF and gain of the LNA plays an important role in determining the NF of the direct conversion receiver.

Three types of linearity parameters are important from a system perspective. These are the input 1dB compression point (ICP), input 3rd order intercept point (IIP3) and input second order intercept point (IIP2). Basic definitions and illustrations are given in [36]. Different linearity conditions are used for different purposes from a system design perspective. They arise from various factors such as in-band blocker, out-of-band blocker, signal crest factor and so on. Both ICP and IIP3 specifications should be known separately, because in some circuits they don't obey the 10dB difference rule. It is important to define the cascaded linearity parameters for the receiver subsystem design.

The cascaded IIP2 is determined by the mixer IIP2 reduced by the LNA gain, since the

LNA doesn't contribute to the IIP2 distortion at baseband. The cascaded IIP3 is given by

$$IIP_3 = \frac{IIP_{3\_mixer}}{\frac{IIP_{3\_mixer}}{IIP_{3\_LNA}} + A^2} \qquad (4.2)$$

Where, IIP3_mixer is the IIP3 of the mixer and IIP3_LNA is the IIP3 of the LNA. From the above equation, if the IIP3 of the LNA is much higher than IIP3 of the mixer, the cascaded IIP3 is the IIP3 of the mixer reduced by the gain of the LNA, similar to the cascaded IIP2. The above equation also suggests that the nonlinearity of the mixer has considerable critical effect on the overall linearity performance of the receiver.

4.3 CONSIDERATION FOR MIXER TOPOLOGY

4.3.1 Design requirements for UWB Mixer

The multiband OFDM system requires less than 6.6dB of receiver noise figure and gain of around 20dB in the RF front-end [13]. Suppose that a LNA can achieve a noise figure of less than 4dB with gain around 12dB, then a mixer should support a gain of more than 10dB with a noise figure of 10dB. A passive mixer also can be considered as a candidate for the UWB receiver. It has good linearity and does not consume DC power, but it has a loss instead of a gain and a poor noise figure. Since the overall linearity of the direct conversion receiver is mainly determined by a mixer, a passive mixer would be a great fit if linearity performance is very important for a system. In this case, a LNA design becomes quite difficult because it should carry the entire gain that would be required for the receiver path. This would require more than a 20dB gain with a very low noise figure for a very wide frequency range in the UWB system, which is quite a

challenge. Furthermore, a passive mixer tends to require a high input power from LO signals. The high power of LO signals can leak into an antenna because of the poor isolation between the RF and LO ports in the passive mixer and result in LO leakage and radiation issues. An active mixer such as a Gilbert cell is well-known for its strong isolation between RF and LO port. It can achieve a reasonable gain with a moderate noise figure.

4.3.2 Double balanced mixer

To prevent LO leakage from reaching the RF output, a double balanced mixer can be used, a solution also known as a Gilbert cell, which is shown in Figure 4.3.

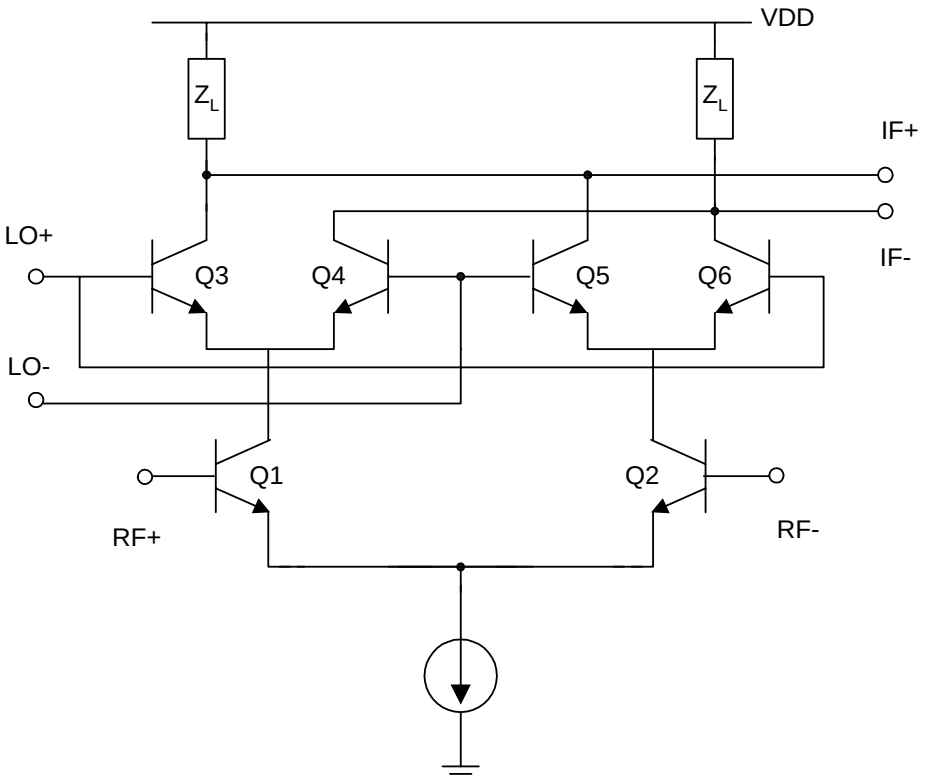


Figure 4.3 Schematic of the double balanced mixer

Assuming the LO drive is large enough to make the differential pairs act like current-steering switches, the schematic shows that the output is connected in a way that the RF signal sums up while the LO signals sum to zero. If care is taken in the layout to minimize mismatches between switching pairs (Q3,Q4,Q5,Q6) and the RF transconductance pairs (Q1,Q2), the IC realizations of this circuit routinely provide 40dB of LO-IF isolation [37], easing filtering requirements at the output.

Assuming that the LO-driven transistors behave as perfect switches, the differential output current may be regarded as the result of multiplying the drain current of Q1 and Q2 by a unit-amplitude square wave. Since the amplitude of the fundamental component of a square wave is 4/π times the amplitude of the square wave, the transconductance of the mixer can be expressed as the following equation.

$$G_m = \frac{2}{\pi} g_m \qquad (4.3)$$

Where g_m is the transconductance of Q1 or Q2.

4.3.3 Noise of Gilbert mixer

To implement direct conversion, two kinds of noise performance should be considered. Namely, flicker noise and the noise figure. In the process of information recovery, a RF signal is down-converted into the baseband through a mixer. However, the mixer itself contributes flicker noise and if there is large flicker noise in the mixer, the down-converted information may be corrupted as shown in Figure 4.4. This problem becomes severe when the device used in the mixer has a large flicker corner frequency in processes such as CMOS or GaAs MESFET. This problem and its solutions have been discussed several times in the literature.. [38,39]. BJT or SiGe HBT has an intrinsically

low flicker noise corner frequency — typically below several hundred hertz — hence, consideration of flicker noise is not a major concern in mixer design.

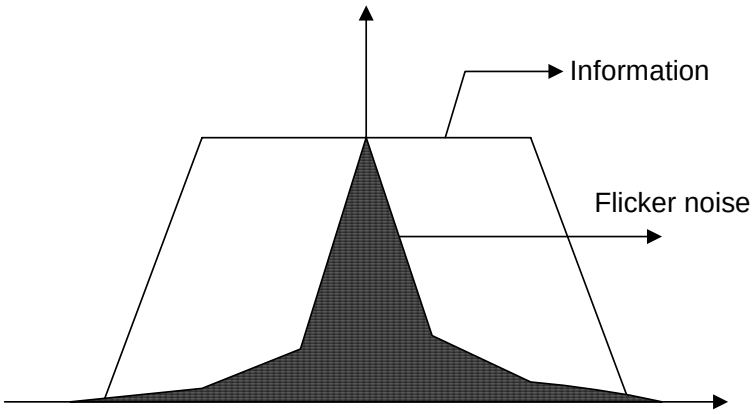


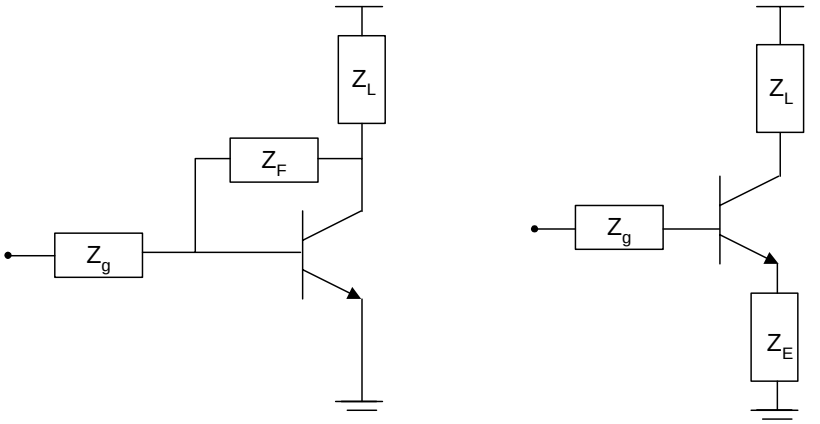
Figure 4.4 The effect of flicker noise on information bearing base-band signal

The noise figure of the mixer should be minimized as a way to give more design freedom to the LNA design with relaxed gain. Q1 and Q2, shown in Figure 4.3, are noise sources in a mixer and affect its noise figure. Basically their noise figure establishes the lower boundary for the noise figure of a mixer. Note that the noise contribution from Q1 and Q2 is proportional to their current consumption because collector shot noise is *2qIc*, which indicates that low DC current is helpful in minimizing the mixer noise figure. However, low DC current would result in low gain and poor linearity of the mixer. One approach to solving this dilemma is to use a high *ft* process. In a high *ft* process such as SiGe HBT, high gain can be obtained with less bias current contributing less noise. Moreover, a certain kind of linearity improvement technique can be used due to high gain [37].

The switching quad pair also degrades noise performance of the mixer in a number of ways. One contributor to the noise figure arises from imperfect switching,

which causes attenuation of the signal current. Therefore, one challenge in such mixers is to design the switches and associated LO drives to provide as little attenuation as possible. Another noise figure contributor associated with switching transistors arises from the interval of time in which both transistors conduct current and hence generate noise. Additionally, any noise in the LO is also magnified during this active gain interval. Minimizing the simultaneous conduction interval reduces this degradation, so to the maximum extent possible, sufficient LO drive must be supplied to make the differential pair approximate ideal, infinitely fast switches.

4.3.4 Linearity of Gilbert mixer



(a) (b)

Figure 4.5 (a) Shunt-feedback topology (b) Series-feedback topology

If the LO-driven transistors behave as good switches, then the linearity of the mixer is mainly determined by its transconductance stage. For a simple technique to

improve the linearity of a transconductor, either series-feedback or shunt-feedback can be used. Representative examples of both types of feedback are shown in Figure 4.5. One of the methods incorporated, series-feedback, is a degeneration technique. For degeneration impedance, a resistor, inductor, or capacitor can be used. Normally, since capacitive degeneration makes the circuit unstable, it has not been popular for use in amplifier design. According to [29], inductive degeneration is the best of the three choices available for improving linearity.. However, an inductor is a frequency dependent component and not well suited for wideband circuit design. Shunt-feedback also can improve linearity by reducing its gain. The operating bandwidth of the circuit is also increased as well in case of shunt-feedback. Both feedback techniques are well-known methods for improving the linearity of an amplifier, yet it is unclear which of them performs best for a given situation.

A Volterra-series analysis provides insight into improvement in linearity performance of the UWB mixer. Eqn.3.25 in Chapter 3 demonstrates that usually IMD3 performance depends on the magnitude of first two items; A and B in Eqn.3.25. So it can be simplified as in Eqn.4.4. Similarly, the Volterra-series analysis of the IMD of series-feedback can be written as in Eqn.4.5, according to reference [29].

$$Shunt\_Feedback\_IMD_3 = \frac{V_T}{3}\left|\frac{G_1(s)}{I_C}\right|^3 \times \left(1 + sC_j Z_g(s) + \frac{Z_g(s)}{Z_F(s) + Z_L(s)}\right) \quad (4.4)$$

$$Series\_Feedback\_IMD_3 = \frac{V_T}{3}\left|\frac{G_1(s)}{I_C}\right|^3 \times \left(1 + sC_j (Z_g(s) + Z_E(s))\right) \quad (4.5)$$

In Eqn.4.4, $Z_g(s)$ includes source impedance as well as the base resistance of the HBT. $Z_F(s)$ and $Z_E(s)$ are shunt-feedback impedance and degeneration impedance in Figure 4.5 (a) and (b) respectively. $Z_L(s)$ is the load impedance in both schematics. Generally, linearity can be improved by increasing a bias current, I_C or reducing gain $G_1(s)$. Suppose $Z_g(s)$ is inductive, $sC_jZ_g(s)$ partially cancels "1" term. The remaining parts that contribute to IMD3 are $sC_jZ_E(s)$ for series-feedback and $Z_g(s)/(Z_F(s)+Z_L(s))$ for shunt-feedback. For realizable values to have a reasonable gain for both schemes, the value of $C_jZ_E(s)$ is on the order of 10^{-12}, while the value of $Z_g(s)/(Z_F(s)+Z_L(s))$ is on the order of 10^{-11}. This indicates that series-feedback is superior to a shunt-feedback scheme for linearity improvement. Furthermore, the transconductance stage of the mixer sees the low impedance of $1/g_m+Z_L/g_mro$ (ro is a resistor depicting finite conductance at the collector) from LO-driven transistors, which results in increasing the value of $Z_g(s)/(Z_F(s)+Z_L(s))$ and causing more degradation in linearity for the shunt-feedback scheme.

Note that Eqn.4.5 does not include $Z_L(s)$ term in the expression of IMD3, which means that load impedance does not affect the linearity of the transconductance in case of degeneration.

So far, we have investigated the linearity of the RF transconductance stage of the mixer when the LO-driven transistors act as good switches. To guarantee good switching, sufficient LO drive is necessary. However, excessive LO drive can result in degradation in linearity because of capacitive parasitic loading on the common-emitter connection of a differential pair [37].

4.4 UWB MIXER DESIGN

The schematic diagram of the designed mixer is shown in Figure 4.6. The mixer incorporated a balun structure at the RF input stage by grounding the other RF port. While an active balun can be used before a mixer to split an RF signal into two differential signals, this configuration reduces any additional power consumption and eliminates any possible noise contribution from the balun. The incorporated balun structure at the RF input stage of the mixer in Figure 4.6 receives a single-ended RF signal and down-converts it into differential IF signals. This approach has little penalty in terms of conversion gain compared with Gilbert cell structure that has differential RF inputs and differential IF outputs as shown in Figure 4.3. The input signals in Figure.4.3 are handled in a differential way. Namely, the input RF differential signals with equal amplitude and 180 degree of phase difference between them are converted to IF signals. If the signal is handled in a differential way, the amplitude of the signals that the transconductance stage can handle with little distortion is bigger than when the signal is handled in single-ended way. Therefore, linearity is improved for the same input amplitude. UWB system specification requires relaxed linearity performance. So in this design, the minimization of power consumption is emphasized more in the design aspect.

Figure 4.6 shows the schematic of the designed UWB mixer. Typically, Q1 and Q2 is the differential pair in the driver stage, which amplifies the RF signal and reduces noise contribution from switching quad (Q3,Q4,Q5,Q6). Since these pairs have an overall impact on the noise performance of the mixer, the size of these pairs should be large for small base resistance; r_b thus achieves low noise performance.

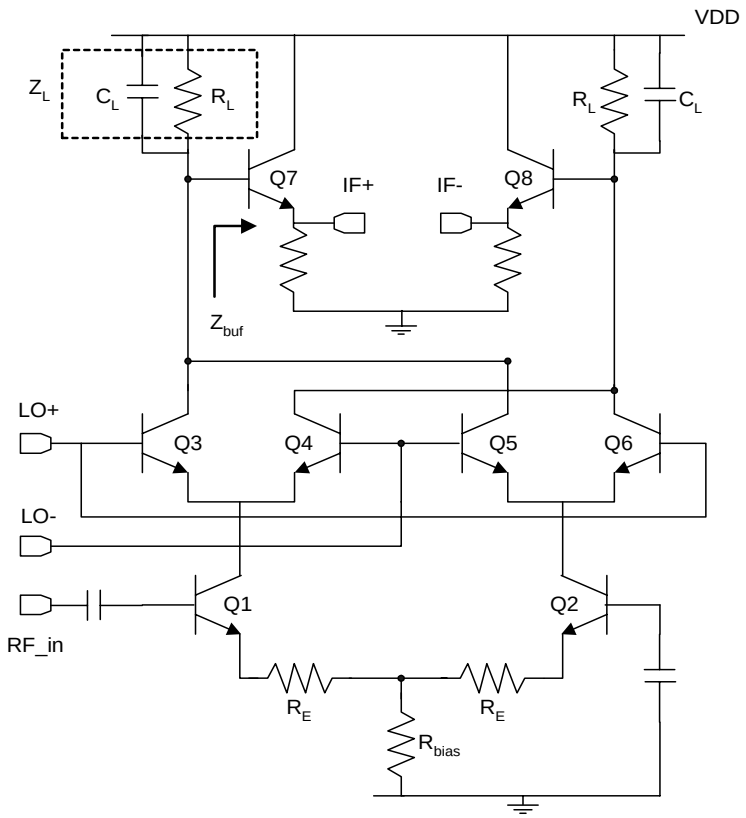


Figure 4.6 Schematic of the designed UWB mixer

The size of the device for Q1 and Q2 is an emitter width of 0.2um and an emitter length of 20um. Since the base resistance, r_b , of the devices Q1 and Q2 is the dominant factor that degrades the noise figure of the mixer, the device with the small emitter width is used to minimize r_b . Even though the emitter length does not affect the noise performance of the mixer, a large emitter length is preferable in order not to degrade linearity performance.

The linearity of the mixer is another important factor. Since the overall linearity performance of the RF front-end receiver chain depends on the linearity of the mixer, the distortion of the mixer should be minimized. Emitter degeneration R_E is used in this

design to reduce the gain while improving linearity performance. By using R_E, the conversion gain of the mixer can be expressed as in Eqn.4.6, assuming perfect switching in LO-driven transistors.

$$Conversion\ gain = \frac{2}{\pi} \cdot \frac{g_m}{1 + g_m R_E} \cdot \left(Z_L \,//\, Z_{buf} \right) \quad (4.6)$$

$$\approx \frac{2}{\pi} \cdot \frac{g_m R_L}{1 + g_m R_E} \quad (4.7)$$

Z_L is the parallel combination of C_L and R_L , and Z_{buf} is the impedance seen from the load to the base of Q7 and Q8. Typically the value of Z_{buf} is much greater than that of Z_L. C_L is used to filter out any unwanted signal, therefore the IF signal only sees R_L as load impedance. Therefore, the Eqn.4.6 can be simplified into Eqn.4.7. Instead of using a current source, the biasing resistor R_{bias} is used to increase voltage headroom, thus improving gain and linearity performance.

The size of transistors in the LO-driven stage should be small to fully switch in response to a small LO signal amplitude. The size for LO-driven transistors (Q3-Q6) was determined through the simulation for the maximum performance in terms of gain, noise and linearity performance. Q7 and Q8 serve as a buffer stage to match 50 ohm at the output. For measurement purposes, the linearity of the buffer stage was designed to be much higher than that of the mixer core. Since the gain of the buffer stage is almost less than one, the noise contribution from the buffer stage is quite less when it is compared with the contribution from the mixer core. All the active transistors are designed to operate in their linear region with proper biasing by ensuring the minimum voltage between collector and emitter so as not to degrade their intrinsic IP3 [27].

4.4.1 Extrapolated results of UWB mixer

The design is fabricated on the 0.18um IBM SiGe HBT BiCMOS process. The design consumes 5mA from a 2.4V power supply. Conversion gain is achieved as 10dB at 3GHz and is reduced to 8.5dB at 10GHz. The noise figure achieved is 8.5dB at 3GHz and is increased to 9.8dB at 10GHz. Its input P1dB is -15dBm at 3GHz. Figure 4.7 shows the fabricated chip photo of the designed mixer. Figure 4.8 shows the extrapolated conversion gain and noise figure of the UWB mixer. The results were calculated from the measured results of the receiver block, which includes UWB LNA and the mixer.

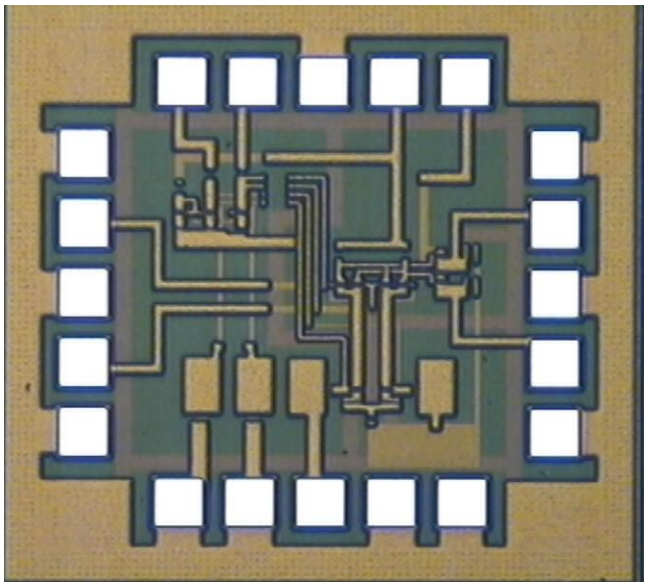


Figure 4.7 The die photo of the fabricated UWB Mixer

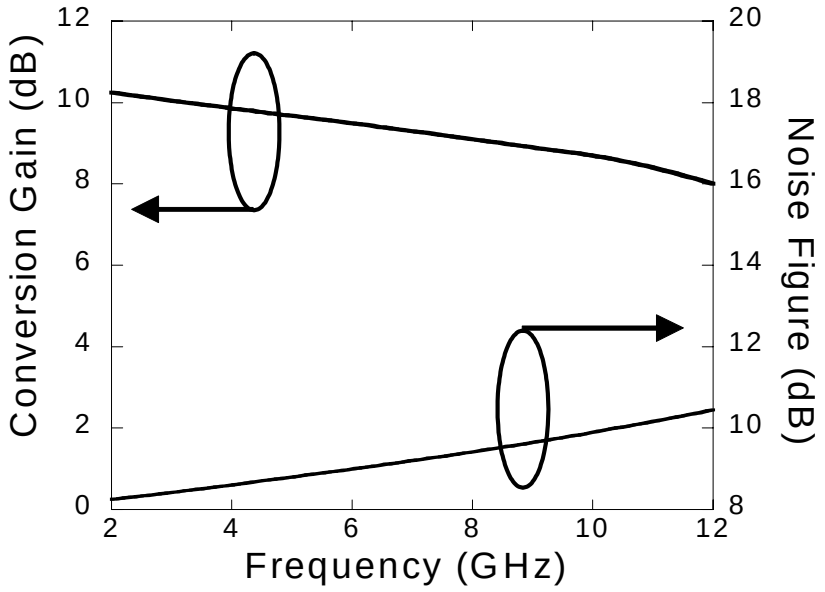


Figure 4.8 Conversion gain and noise figure of the UWB mixer along with frequency

4.5 UWB DIRECT CONVERSION RECEIVER DESIGN

The main concerns of the design of UWB receiver are as follows: First, in order to achieve the required bit rate up to 110Mbps at 10m distance, the MB-OFDM system maximizes the bandwidth usage and reduces the implementation margin. This means that the loss associated with all the components from an antenna to a mixer should be minimized. The input matching between RF passive components and the LNA should be good for a very wide bandwidth to reduce loss as well. Second, the general understanding of the operation of a wideband circuit is that the circuit tends to consume more power to achieve a wideband operation. Another concern would be that a narrowband resonating technique [22] to reduce power consumption is not applicable to a wideband circuit design. Considering these concerns, it is a challenge to implement a UWB receiver that will have low DC power consumption, meet all the required specifications, and have little

input return loss over full UWB bands.

4.5.1 Circuit design

The resistive feedback UWB LNA is integrated with the mixer. A slight modification was made, but the basic principles for LNA design remain the same as described in Chapter 3. The receiver design uses a transmission line inductor between the LNA and the mixer to eliminate the null point. The use of this inductor not only ensures gain over the UWB frequency bands but also helps to improve the linearity of the mixer. This can be understood easily from Eqn.4.5. In Eqn.4.5, $Z_g(s)$ is source impedance. When an inductor is used between the LNA and mixer, the RF port of the mixer sees inductance, which partially cancels "1" term in $(1+sC_j(Z_g(s)+Z_E(s))$. Therefore, the linearity improvement can be observed especially at high frequencies. Special care was taken to ensure that overall linearity undergoes little degradation and current consumption is minimized. The main focus of the design was concentrated on minimizing the noise figure of the receiver and obtaining the required gain of at least 20dB over the frequency range of 3-10GHz. Figure 4.9 shows the implemented block of the receiver.

4.5.2 Measured results of the UWB receiver

The design was fabricated on IBM 0.18um 120GHz SiGe HBT BiCMOS process. Figure 4.10 shows the chip photo of the fabricated design. The size of the design is 1250um x 1800um including pads. The design consumes 11mA from a 2.4V power supply. The measured input return loss is less than 9.5dB over full UWB bands, which is from 3.1GHz to 10.6GHz.

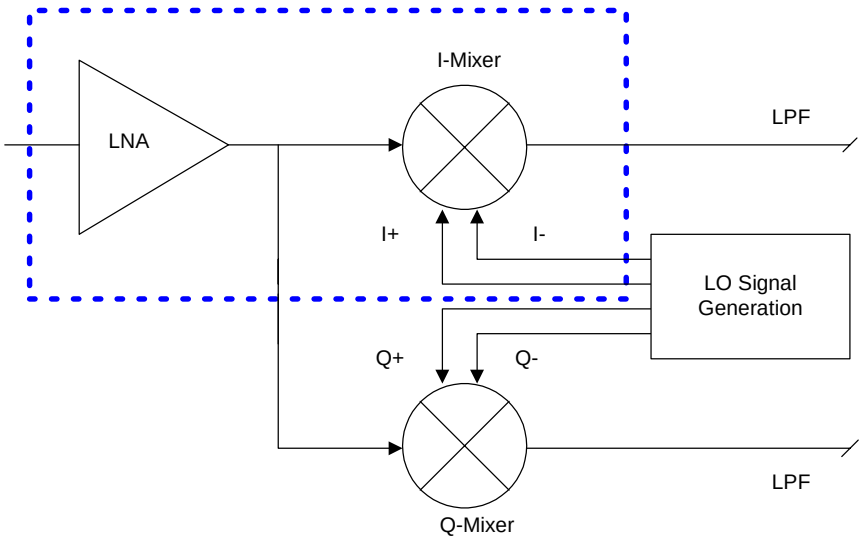


Figure 4.9 Implemented block of the UWB receiver.

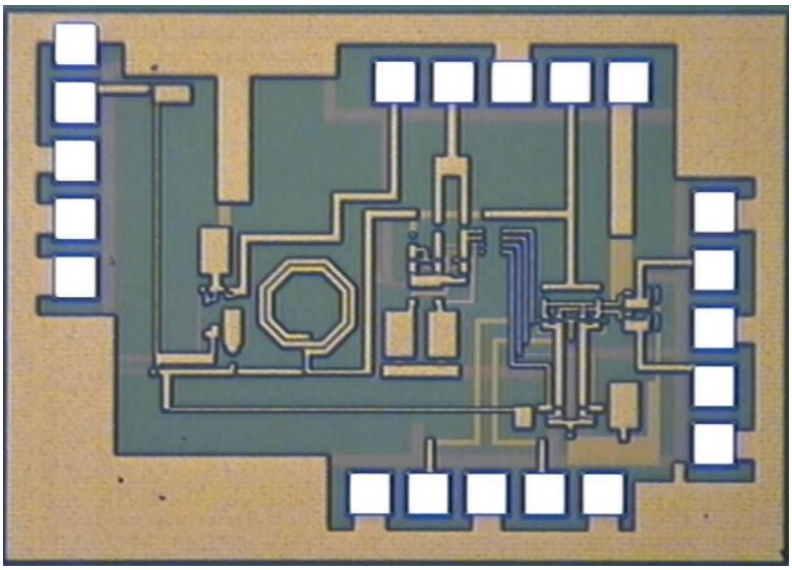


Figure 4.10 The chip photo of the fabricated UWB receiver

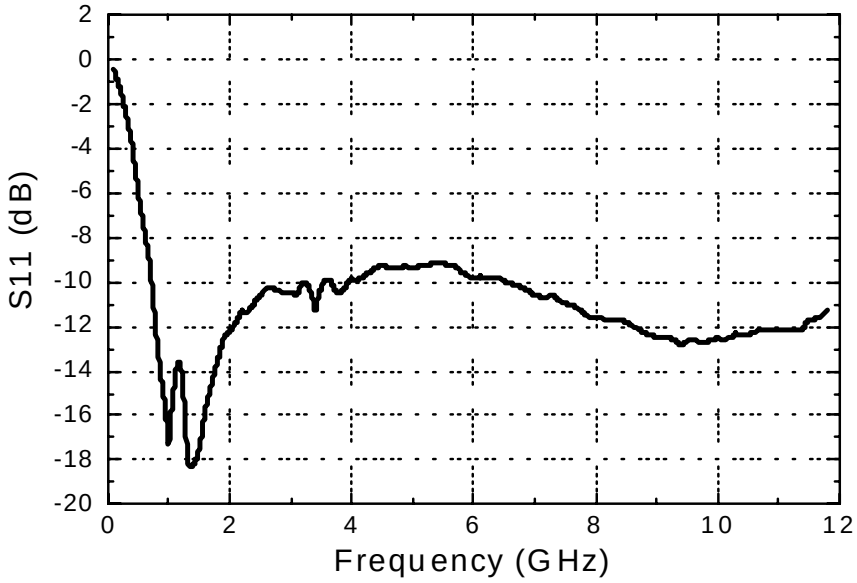


Figure 4.11 Measured input matching of the receiver

The measured gain and noise figure of the receiver is shown in Figure 4.12. The gain of the receiver was a measured 25dB at 3GHz and was reduced to 20.5dB at 10GHz. The gain reduces as frequency increases. This is because the conversion gain of the mixer decreases as frequency increases. Compensation by placing an inductor between the RF transconductance stage and the switching stage in the mixer would improve this decrease of gain. However, because the gain flatness over the 500MHz channel is more important than full band gain flatness, this drop in gain can be compensated for as long as the gain is flat over the 250MHz frequency ranges from DC.

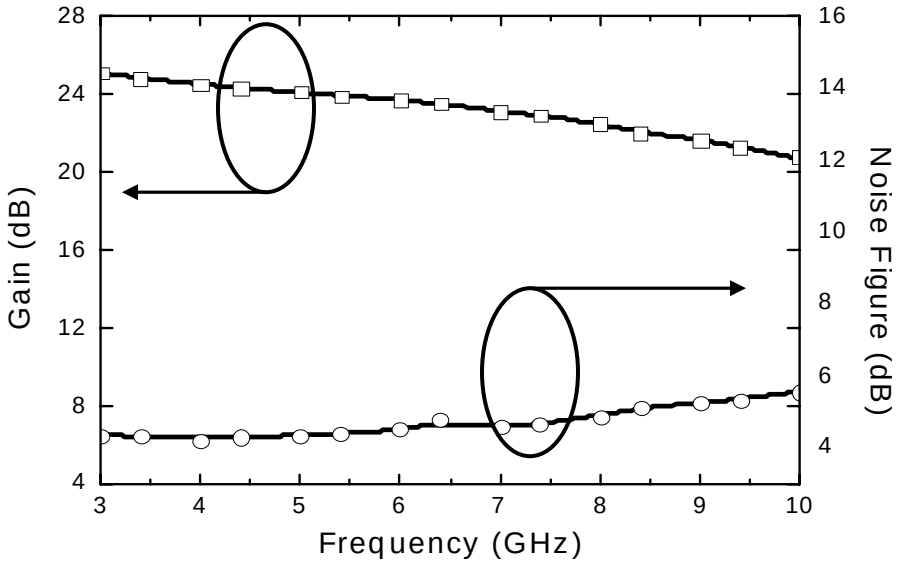


Figure 4.12 Measured gain and noise figure of the UWB receiver.

The noise figure was a measured 4.5dB at 3GHz and increased to 5.8dB at 10GHz. The increase of the noise figure at high frequency is because the device's intrinsic noise tends to increase at high frequency, and the gain of LNA drops at high frequency, thereby increasing the noise contribution from the mixer. Both gain and noise figure performances are met for the target specifications. Figure 4.13 shows the conversion gain measured at each frequency point, along with the LO input power.

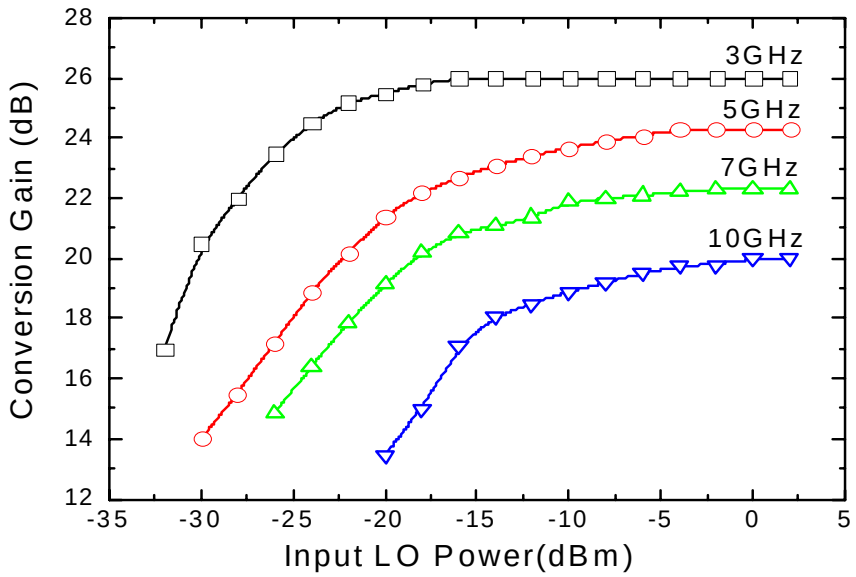


Figure 4.13 Conversion gain vs input LO power measured at each frequency

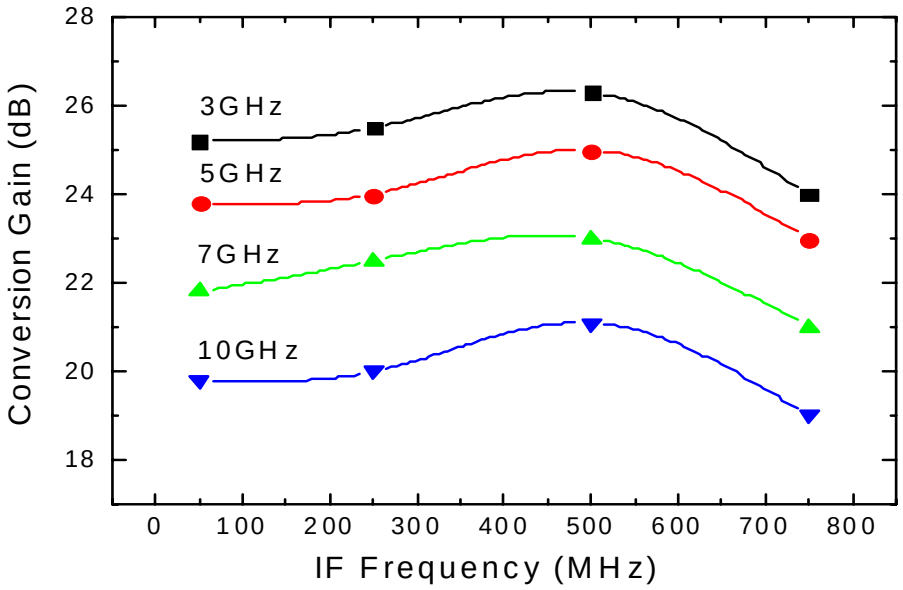


Figure 4.14 Conversion gain vs. IF frequency

As can be seen in Figure 4.13, a proper LO input power is required to have a stable conversion gain. At the low frequency of 3GHz, the input LO power of as low as -17dBm is enough for the receiver to achieve gain of around 25.5dB. However, at the high frequency of 10GHz, LO input power of at least 0dBm should be applied to the receiver to obtain gain of more than 20dB. This is primarily because efficient switching in the LO-driven stage becomes harder as frequency goes up.

Figure 4.14 shows conversion gain along with IF frequency at the input LO power of 0dBm. System specifications require a flat gain from DC to 264MHz to accommodate channel bandwidth of 528MHz. A simulation showed a flat gain up to 1GHz IF frequency. However, the measurement in Figure 4.14 shows that there is a gain that peaks at around 500MHz IF frequency. This kind of peaking phenomenon comes from the resonance of inductance and capacitance. Because the resonant frequency is relatively low, the suspected cause of this peaking is the large value of the inductor and capacitor used in the DC-bias tee in the measurement setup. The measured gain deviation up to the IF frequency of 264MHz is less than 0.5dB.

A two-tone test was applied with a signal spacing of 100MHz to measure the linearity performance of the receiver. The linearity is measured at 3, 5, 7 and 10GHz to ensure the performance over full-band UWB frequency ranges. The linearity performance of the designed receiver is shown in Figure 4.15, 4.16, 4.17, 4.18. for each measured frequency. The measured input P1dB is -23dBm at 3GHz. The input P1dB is improved as the frequency increases because of less gain at high frequencies and the increased cancellation effect of inductance at the input of the transconductance stage of the mixer. The input P1dB of -19dBm is measured at 10GHz. IIP3 of -11dBm was measured at

3GHz, which increases up to -7dBm at 10GHz. IIP2 of +27dBm was measured at 3GHz, which also increases up to +40dBm at 10GHz. The linearity performance of the receiver is summarized in Figure 4.19.

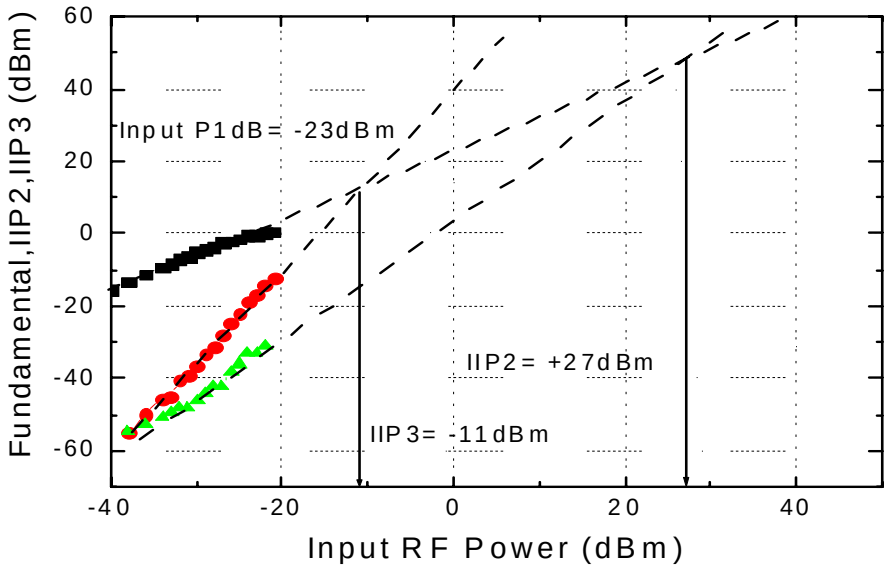


Figure 4.15 Measured input P1dB,IIP3 and IIP2 at 3GHz

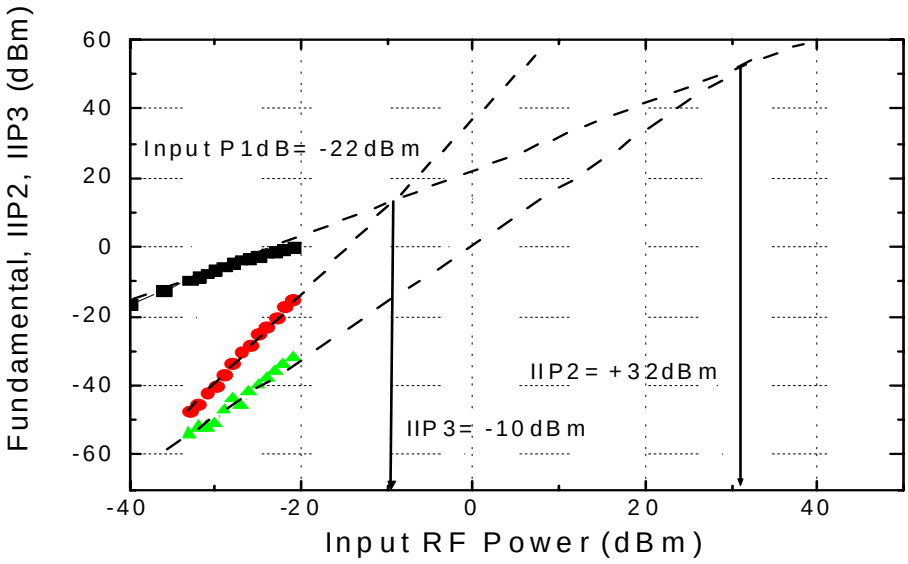


Figure 4.16 Measured input P1dB, IIP3 and IIP2 at 5GHz

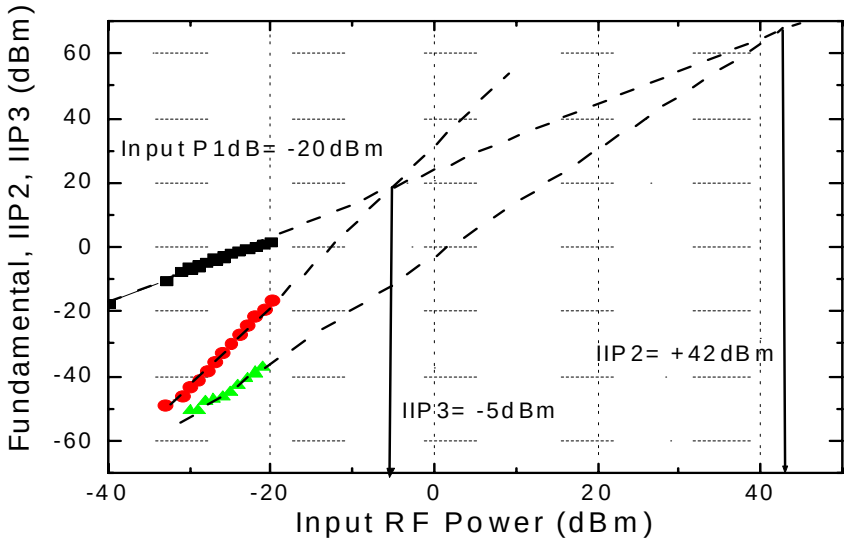


Figure 4.17 Measured input P1dB, IIP3 and IIP2 at 7GHz

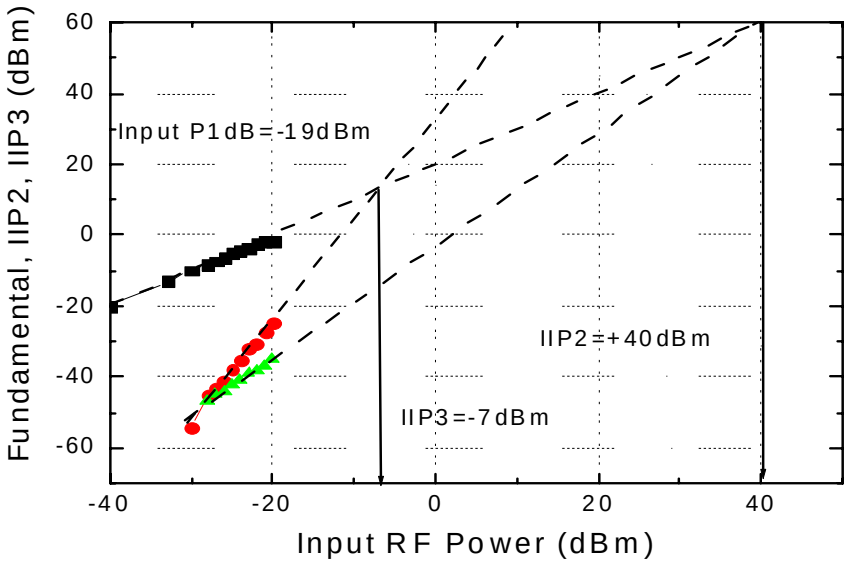


Figure 4.18 Measured input P1dB, IIP3 and IIP2 at 10GHz

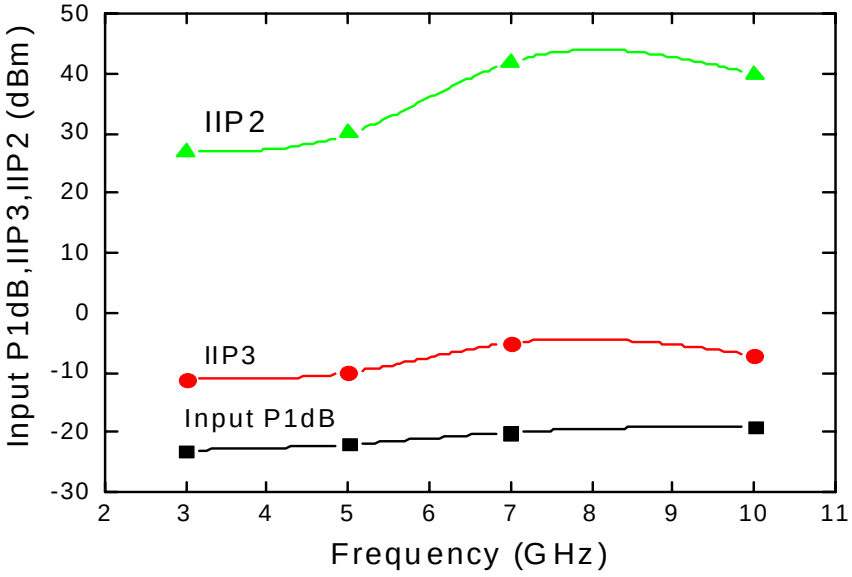


Figure 4.19 Input P1dB, IIP3, IIP2 of UWB receiver vs. frequency

Figure 4.19 shows the overall linearity performance of the receiver. Overall linearity including input P1dB, IIP3, and IIP2 improves as the operating frequency increases.

LO-RF and LO-IF isolation are shown in Figure 4.20. More than 60dB of LO-RF isolation was measured. LO-IF isolation was measured between 25 and 30dB over the entire band. Relatively low LO-IF isolation comes from device mismatches of the mixer; however, the LO signal component at the IF stage can be filtered out by using a low-pass filter. The measured results of the UWB receiver are summarized in Table 4.2.

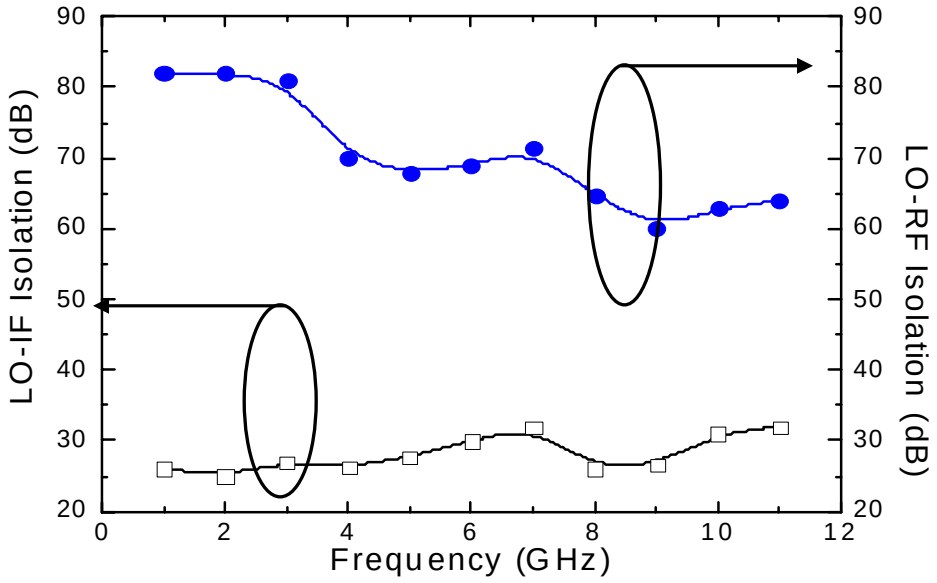


Figure 4.20 LO-RF and LO-IF isolation vs frequency

Table 4.2 Summarized results of the UWB receiver

	Performance of the UWB receiver
Gain	25 – 20.5 dB
Noise figure	4.5 – 5.8 dB
Operating bandwidth	3 – 10GHz
Input return loss	Less than -9dB over the entire UWB bands
Input P1dB	>-23dBm
IIP3	>-11dBm
IIP2	>27dBm
Power consumption	11mA from 2.4V supply
Technology	0.18um IBM SiGe HBT BiCMOS

CHAPTER V

WIDEBAND CMOS VCO DESIGN

5.1 OVERVIEW OF OSCILLATOR OPERATION

As demand in the commercial market increases for dual-band or ultra-wideband wireless communication applications that combine low cost, low power consumption and high data rates, the design of wideband circuits becomes an essential part in the search for a solution that meets these goals. In the past, most of the RF front-end was designed to meet the requirements of narrowband wireless applications such as GSM, WCDMA and wireless LAN. However, today's trend is toward multiband and multimode applications, which utilize wider bandwidth to support a higher data rate or to incorporate two or three standard wireless communications to expedite the convenience of the user for the different solutions. This trend requires a wideband VCO that can cover the frequency range of the system in question. An oscillator is the most critical part in modern circuit design because most of the reliable systems are synchronous, which require clean clock sources. As IC technologies and theories regarding the phase noise of a VCO have advanced, on-chip clock sources for wireless applications have become feasible and are integrated with other analog and digital circuitry. Phase-noise is generally characterized in the frequency domain. In a practical oscillator, the output is more generally given by

$$V_{out} = V_0(t) \cdot f[\omega_0 t + \phi_0(t)] \quad (5.1)$$

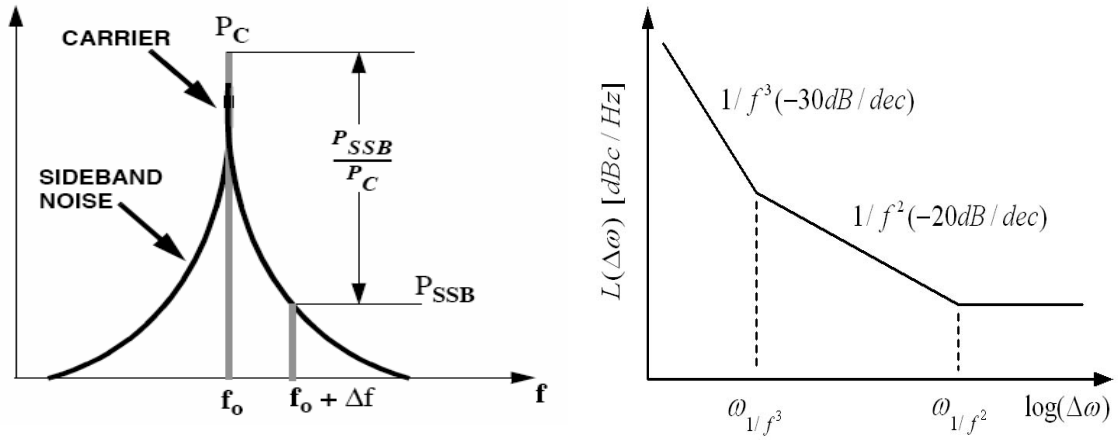
where $V_0(t)$ and $\phi_0(t)$ are functions of time and f is a periodic function that represents the steady-state output waveform of the oscillator. The output spectrum has power

harmonics of around ω_0 if the waveform, f, is not sinusoidal.

As a consequence of the random fluctuations represented by $V_0(t)$ and $\phi_0(t)$, the spectrum will have sidebands close to the oscillation frequency, which is phase-noise as shown in Figure 5.1. To quantify this phase noise, we consider a unit bandwidth (1Hz) at an offset of $\Delta\omega$ from the carrier, calculate the noise power in the band, and divide this result by the carrier power. This is the single-sided spectral noise density in units of dBc/Hz as

$$L(\Delta\omega) = 10 \cdot \log\left[\frac{noise\ \ power\ in\ a\ 1Hz\ bandwidth\ \ at\ \ frequency\ \ \omega_0 + \Delta\omega}{carrier\ \ power} \right] \quad (5.2)$$

Spectral density is usually specified at one or a few offset frequencies. To be a meaningful parameter, both the noise density and the offset frequency need to be included.



(a) Definition of phase noise (b) Phase noise of a general oscillator

Figure 5.1 Phase noise of an oscillator

5.2 EFFECT OF PHASE NOISE IN WIRELESS SYSTEM

In an ideal case, a LO signal can be expressed as an impulse in the frequency domain, and the RF signal is down converted to a lower frequency without any signal distortion. However, in reality, the desired signal may encounter substantial interference in an adjacent channel, and the LO signal itself contains phase noise as shown in Figure 5.2. When these two signals are mixed with the LO output, the down-converted signal will consist of two overlapping spectra. The desired signal suffers from significant noise because of the tail of the interferer, which is called "reciprocal mixing" [36].

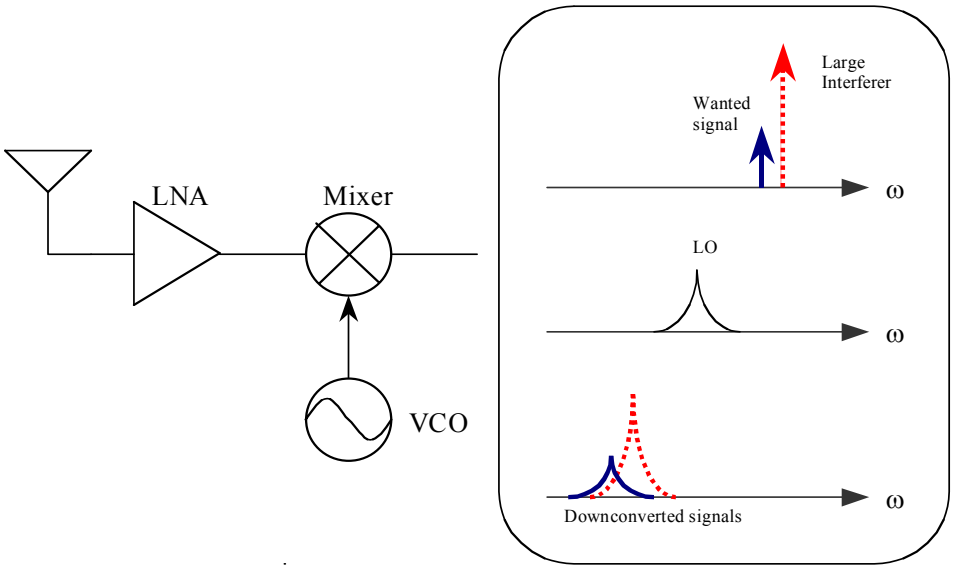


Figure 5.2 Reciprocal mixing effect of phase noise in a practical system

5.3 PHASE NOISE THEORY

The most famous model of the phase noise of an oscillator was suggested by Leeson [40] in 1966. Although this is an empirical expression, the model contains critical factors

that can help to understand the logic behind the mysterious phase noise of an oscillator. According to the model, phase noise can be expressed in Eqn 5.3.

$$L(\Delta\omega) = 10 \cdot \log\left[\frac{2FkT}{P_S} \cdot \left[1 + \left(\frac{\omega_0}{2Q_L \cdot \Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \qquad (5.3)$$

where F is an empirical parameter, k is Boltzman's constant, T is the absolute temperature, P_s is the average power dissipated in the resistive part of the tank, ω_0 is the oscillation frequency, Q_L is the effective quality factor of the tank with all loading accounted for, $\Delta\omega$ is the offset from the carrier, and $\omega_{1/f3}$ is the frequency of the corner between $1/f^2$ and $1/f^3$ the region as shown in Figure 5.1(b).

After Adler studied locking phenomena in oscillators in 1943 [41], Kurokawa published a paper on a synchronized oscillator in which he introduced AM and FM noise components in the analysis of phase noise [42]. In his paper, Kurokawa demonstrated that FM noise can be considerably lessened by synchronization but the AM noise degrades slightly, findings that introduced the theoretical background for the concept of injection locking that is still used. Although Leeson's model can describe and predict the overall phase noise of an oscillator, the model has a fitting parameter, such as F, that makes accurate phase noise prediction difficult.. Another problem is that the model is based on the Linear Time Invariant (LTI) system but the principle of an oscillator's operation is based on nonlinear time varying. The need for an accurate model of phase noise hastened the research on the theory of phase noise and resulted in numerous theories that tried to describe the behavior of an oscillator in a nonlinear way. A Linear Time Variant (LTV)

model is suggested to overcome the limitations of the previous theories and to give design insight [43]. Although the fundamental property of an oscillator is nonlinear time varying because of its amplitude limiting, the LTV model assumes that amplitude-control nonlinearities do not affect phase noise, and therefore, linearity can be a reasonable assumption as far as the noise-to-phase transfer function is concerned.

In the LTV model, the amount of noise that an active device and a resonator contribute to the phase noise of an oscillator depends on where the action happens. If an impulse is applied at the peak of the voltage across the capacitor, no phase shift will occur and only an amplitude change will result. On the other hand, if this impulse is applied at the zero crossing, it has a maximum effect on the excess phase, $\phi(t)$, and a minimum of effect on the amplitude, as depicted in Figure 5.3. This relation is defined as the impulse sensitivity function (ISF) because it determines the sensitivity of the oscillator to an impulsive input.

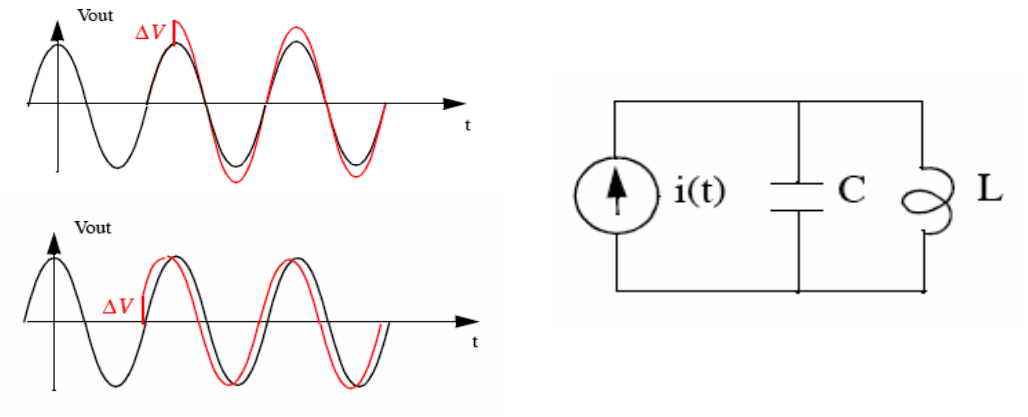


Figure 5.3 Linear Time Varying model

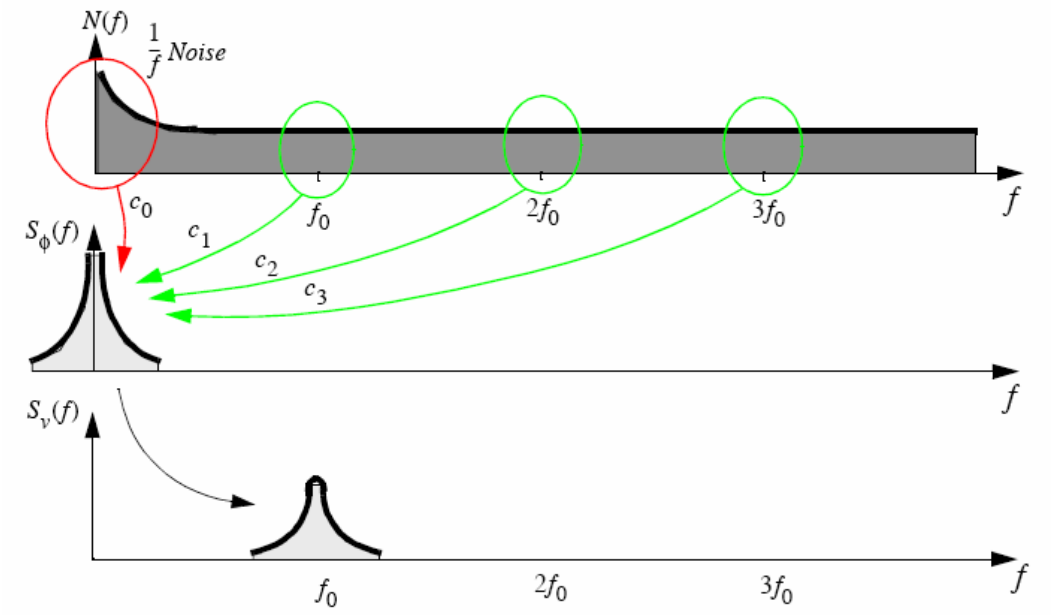


Figure 5.4 Noise conversion process in LTV model

According to the model, the tones in the vicinity of integer multiples of f_o are converted to phase noise with an offset of Δf. Because C_0 is the conversion coefficient for flicker noise upconversion, phase noise from a large flicker noise device, such as a CMOS or GaAs MESFET, can be reduced by reducing coefficient C_0. The coefficient C_0 is related to the waveform of an oscillator. The symmetric rising and falling edge has a lower C_0 value than an asymmetric waveform; therefore by designing an oscillator to have a symmetric waveform, flicker noise upconversion can be reduced, which results in low phase noise in the CMOS or GaAs MESFET process.

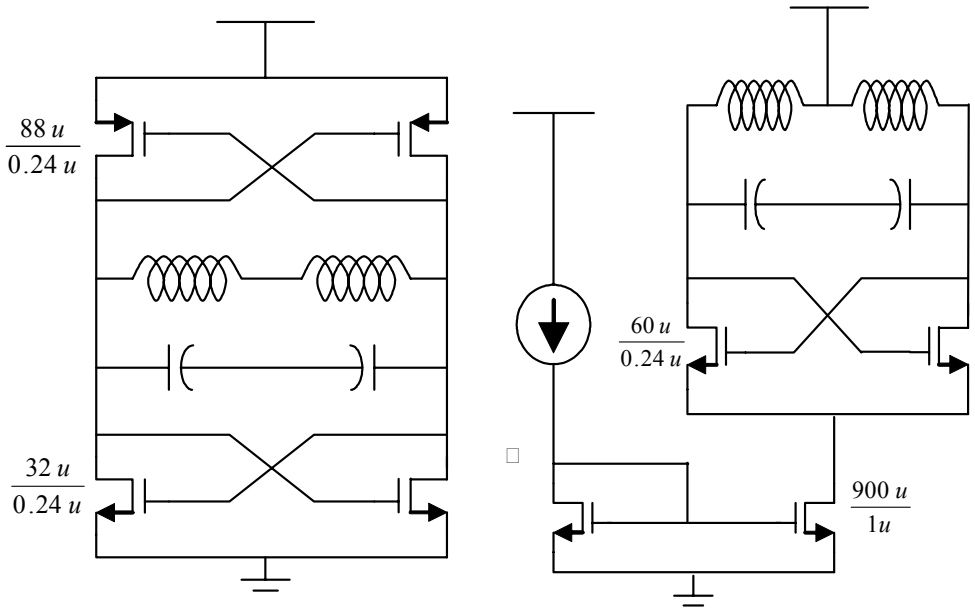
5.4 DESIGN AND COMPARISON OF WIDEBAND CMOS VCOS

Since a CMOS device has a large flicker corner frequency, the design of a CMOS VCO has been a challenge. Two VCO topologies are compared in terms of tuning range and

phase noise performance in the tuning range. Several factors reduce the tuning range of a VCO. These factors include the parasitic capacitances of inductors and capacitors and the size of active devices. The upper boundary of the tuning range is restricted by the parasitic capacitances of the circuit and the inductance value that is required to meet the amplitude and phase noise specification. In order to meet the specifications for the given power consumption, a cross-coupled VCO with a current source is usually used in the CMOS IC design. The advantage of this topology lies in its symmetric waveform, which leads to a reduction in flicker noise up-conversion [43], and since it uses a current source, to less oscillation frequency variation caused by supply voltage.

The transconductance (*gm*) of the above topology is determined by the current consumption and by the geometry of the devices. Since this topology reduces voltage headroom because of the presence of a current source, a large device is needed to get enough *gm* to start an oscillation; the large device then increases the parasitic capacitances, which, in turn, result in reduced tuning range. This problem becomes severe as the supply voltage tends to drop.

Recent reports in the literature showed that the noise generated from the current source can be reduced by on and off chip filters [44], but this still fails to solve the problem of reduced tuning range associated with this topology. Several papers have been published on a cross-coupled VCOs without a current source and have emphasized their good phase noise performance [45]. Moreover, a cross-coupled VCO without a current source has another advantage, a large achievable tuning range. Since this provides relatively large voltage headroom, the small size of the device can get enough *gm* to start an oscillation, which results in a large tuning range.



(a) (b)

Figure 5.5 (a) VCO without a current source :NP_VCO (b) VCO with a current source: N_VCO

Two VCO topologies shown in Figure 5.5 (a) and (b) are designed and measured with the same current consumption and the same size of varactor. These two topologies were selected to meet a wide tuning range for given conditions, such as power supply and current consumption. The chip is designed in a standard digital 0.25um CMOS process. The process has five metal layers, and the substrate resistivity is 10ohm-cm. The thickness of the top metal is less than 1um.

For NP_VCO in Figure 5.5(a), NMOS and PMOS devices are scaled to have the same transconductance to get a symmetric waveform, which results in reduced up-converted flicker noise. For N_VCO in Figure 5.5(b), the NMOS devices are scaled to provide the

minimum gain required to start an oscillation, which will enable this topology to have a comparable wide tuning range.

Two 1.2nH of inductors are used in both designs. One way of achieving a high Q inductor in the CMOS process is to use a patterned ground shield (PGS) under the inductor layout [46]; however, since using PGS adds more parasitic capacitances, this reduces the tuning range. Therefore, to reduce parasitic capacitances, the inductors used in the design use stacked metal5 and metal4 without PGS. . The measured and de-embedded result for the inductor shows a Q of 3.5 around the designed oscillation frequency. The results are shown in Figure 5.6.

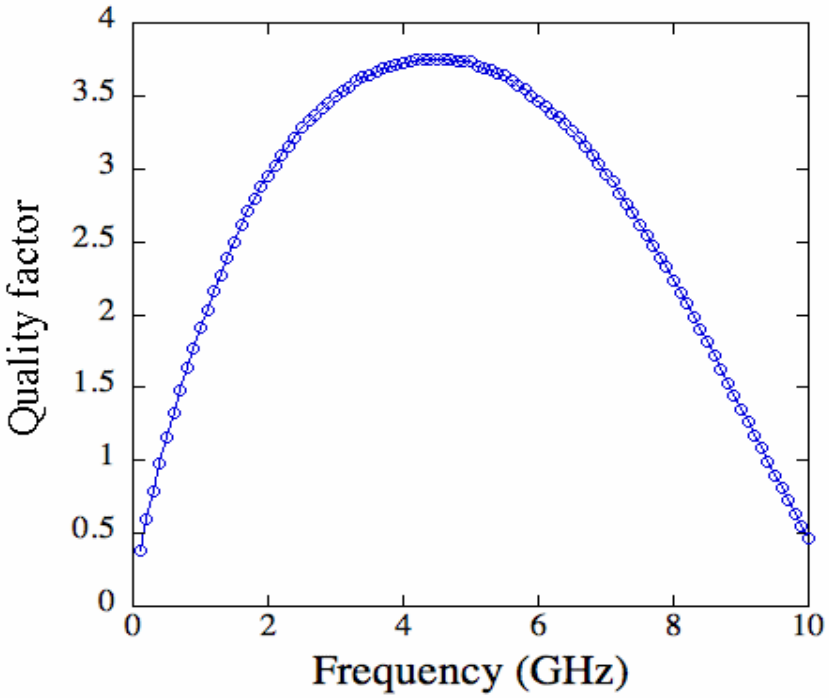


Figure 5.6 De-embeded quality factor of the inductor

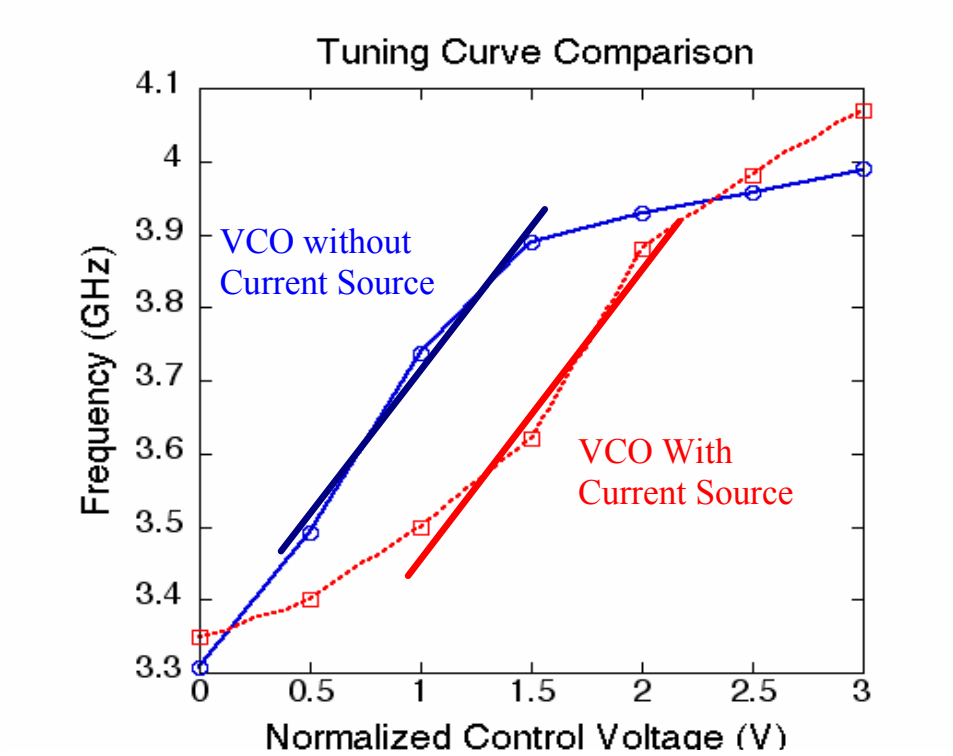
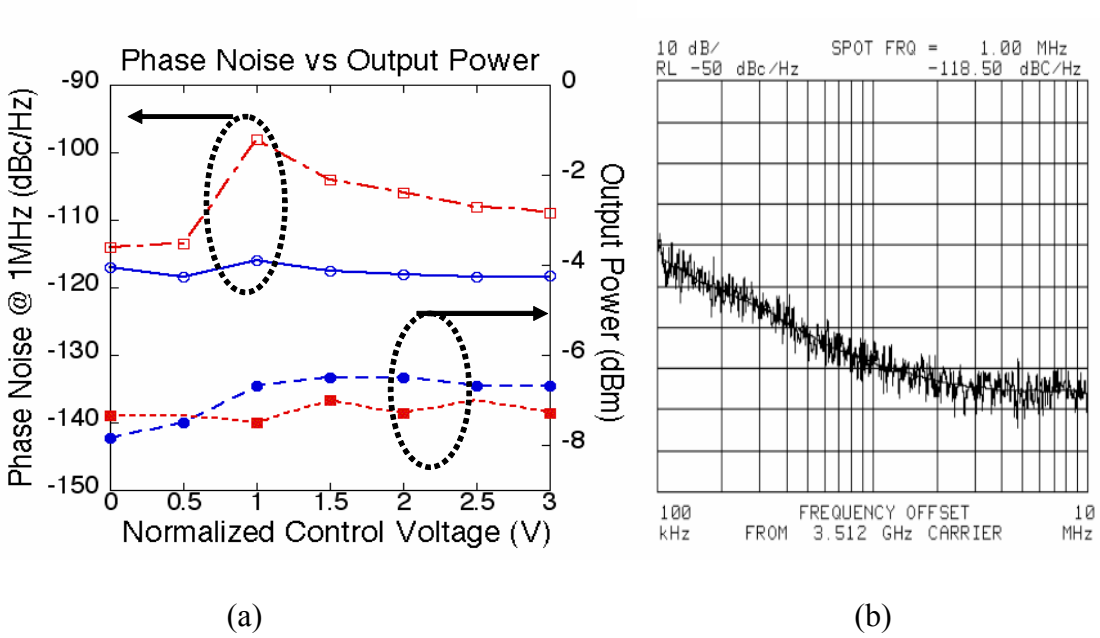


Figure 5.7 Tuning curve comparison between two VCOs

MOS-varactors are used in a strong inversion mode to vary the frequency of interest. With the help of a phase noise measurement kit in a free running state, two VCOs were measured using a spectrum analyzer (8565E). Figure 5.7 shows the tuning characteristics for both topologies. The NP-core VCO without a current source (NP_VCO) is tuned from 3.3GHz to 3.95GHz, and N-core VCO with a current source (N_VCO) is tuned from 3.34GHz to 4.07GHz. Maximum varactor gain for NP_VCO is 500MHz/V, and 600MHz/V for N_VCO. The measured tuning range for the two VCOs indicates that both topologies are compatible.

The comparison of measured phase noise performance is shown in Fig.10(a), along with the tuning range. NP_VCO achieves up to –118.5 dBc/Hz at 1MHz offset of phase

noise with 2dB of variation across the whole tuning range, whereas N_VCO achieves at best –114 dBc/Hz at 1MHz and up to 17dB of phase noise degradation. The main reason for the large amount of phase noise degradation for N_VCO is that because of high steep varactor gain [45], AM noise from the current source is converted into phase noise through the AM-FM conversion process. Since NP_VCO lacks a current source and was operated in a voltage limited region, it doesn't show AM-FM conversion in the tuning range and therefore yields flat phase noise performance. The designed NP_VCO achieves 18% of the tuning range, while the N_VCO achieves 20% of the tuning range.



(a) (b)

Figure 5.8 Phase noise performance of two VCOs (a) Phase noise comparison between two VCOs (b) Phase noise measured for a VCO without a current source

The performance of the fabricated VCO can be compared with others in the literature using the Figure of Merit (FOM) expression in the reference [47]. The FOM is calculated considering phase noise, oscillation frequency, power consumption and tuning range as

shown in Eqn 5.4. The previously published works in a standard CMOS process are compared, and the result is shown in Figure 5.9.

$$FOM = 10\log(L\{\Delta w\}) - 10\log\left(\left(\frac{w_o}{\Delta w}\right)^2 \frac{1}{P}\right) - 10\log\left(\frac{Tuning}{V}\right) \qquad (5.4)$$

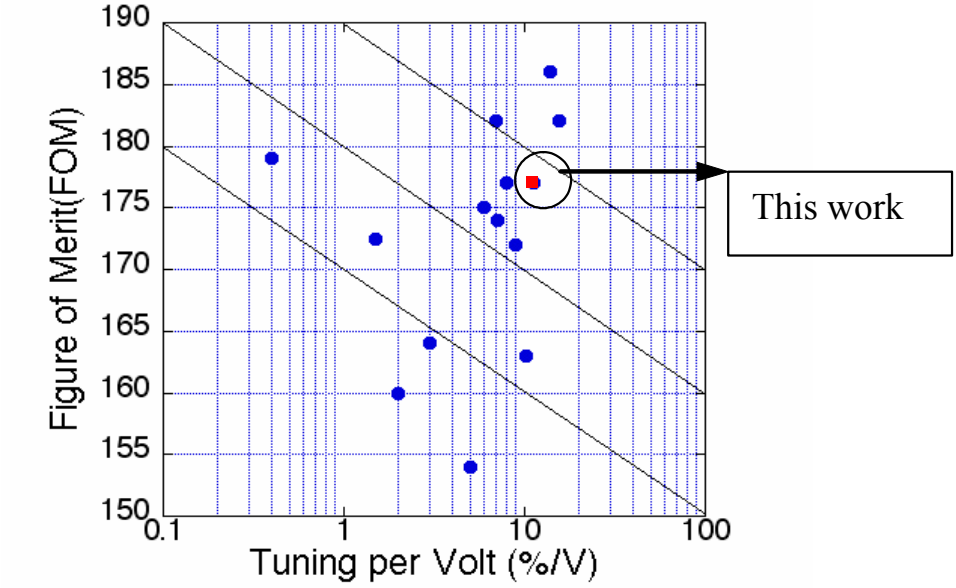


Figure 5.9 FOM comparison

Photographs of the fabricated chip are shown in Figure 5.10, along with a schematic diagram of the comparison of the VCOs. An inductor is inserted in the N_VCO between the core transistors and a current source to reduce up-converted noise from the current source.

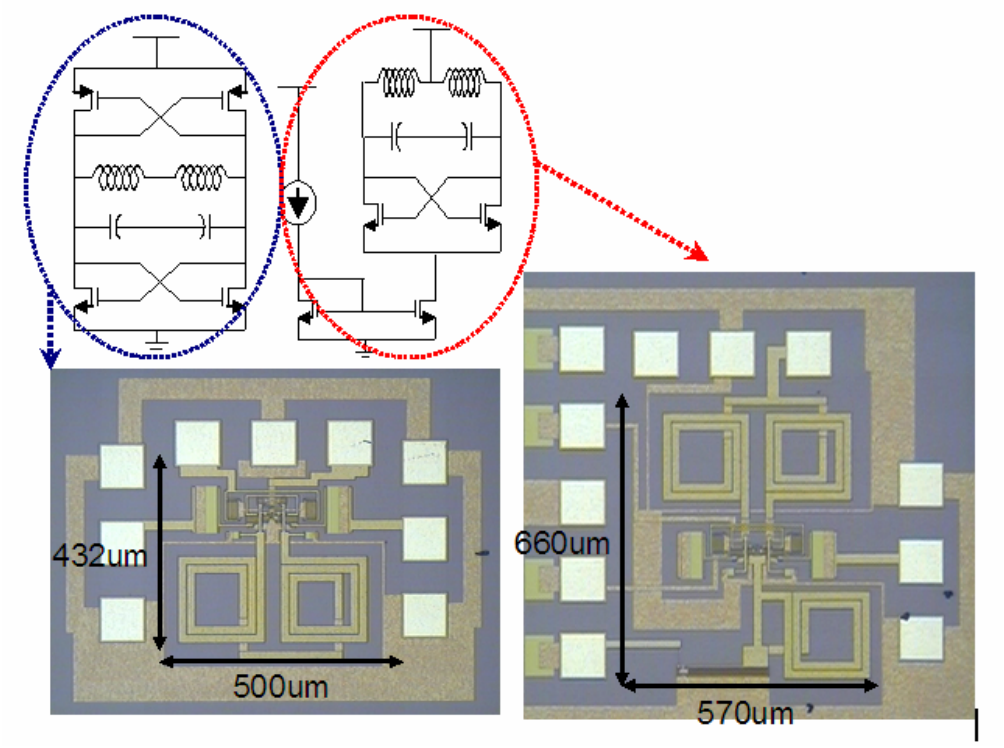


Figure 5.10 The photos of the fabricated VCOs

5.5 SUMMARY OF THE EXPERIMENT

In this chapter, one of the factors critical to performance in wideband applications, the phase noise of a VCO in the wide tuning range was investigated. Two VCOs using different topologies were designed and fabricated for the investigation of wide-band tunability and low phase noise operation in the tuning range. The measured performance of the two VCOs shows that the NP-core VCO outperforms the N-core VCO because of its elimination of a current source. Although the NP-core VCO shows better phase noise results, the performance of a VCO depends heavily on process variation because it lacks a current source. The power consumption of such a VCO can vary up to three times from each process corner. High varactor gain, which is inevitable with a wide tuning range, causes a PLL to take a rather long time to get a lock, resulting in long transient time for

switching bands in a system.

CHAPTER VI

FRACTIONAL LO SIGNAL GENERATOR

FOR THE GSM/WCDMA DUAL-BAND APPLICATION

6.1 LO SIGNAL GENERATION FOR DIRECT CONVERSION ARCHITECTURE

In wideband systems such as the UWB or GSM/WCDMA dual-band system, proper LO signal generation is the most important issue because it must cover a wide frequency range and consume very little power in doing it. Most current wireless services use Quadrature Phase Shift Keying (QPSK) or a variation of this modulation scheme to support their data transfer protocols. This modulation scheme requires I and Q signal separation and demodulation to fully recover the information. Although heterodyne receivers use simple polyphase circuitry to perform phase differentiation with great accuracy at much lower IF frequencies , homodyne receivers perform the same function at higher frequencies, leading to a very challenging task of implementing accurate phase shifters.

Extraneous DC voltages in the demodulated spectrum of a direct conversion receiver not only corrupt the output, but also propagate through baseband circuitry and saturate the subsequent stages. These DC offsets are mostly generated through self-mixing of the LO signal and through mismatches in the mixer [3,4]. In a direct conversion receiver (DCR), the mixer is immediately followed by LPFs and a chain of high gain direct-coupled amplifiers that can amplify small levels of DC-offset and saturate the stages that follow. Consequently, the sensitivity of the receiver can be directly limited by the DC-offset component of the mixer output.

The main problems associated with the design of LO signal generation that can degrade the performance of a transceiver are DC-offset generated from LO leakages, LO pulling because of high output power from a power amplifier (PA), and I/Q mismatches.

6.1.1 LO signal generation scheme for reduced DC-offset and LO-pulling effect

Generally, the DC-offset can be separated into two components, a constant and a time varying offset. The constant DC-offset can be attributed to mismatches between mixer components, while the time varying DC-offset is generated by the self-mixing of the LO as demonstrated in Figure 6.1. Because of imperfect isolation between the LO and the RF ports of the mixer, a finite amount of LO leakage into the RF port persists. In addition, LO leakage and even LO radiation can reach the low noise amplifier (LNA) or other stages prior to the mixer and propagate through the front-end. These signals can get amplified before arriving at the mixer and bring about a serious issue of self-mixing that results in the generation of a relatively large DC component at the mixer outputs. The level of this DC-offset, which is dependent on the time-varying load of the antenna, can also vary with time [4].

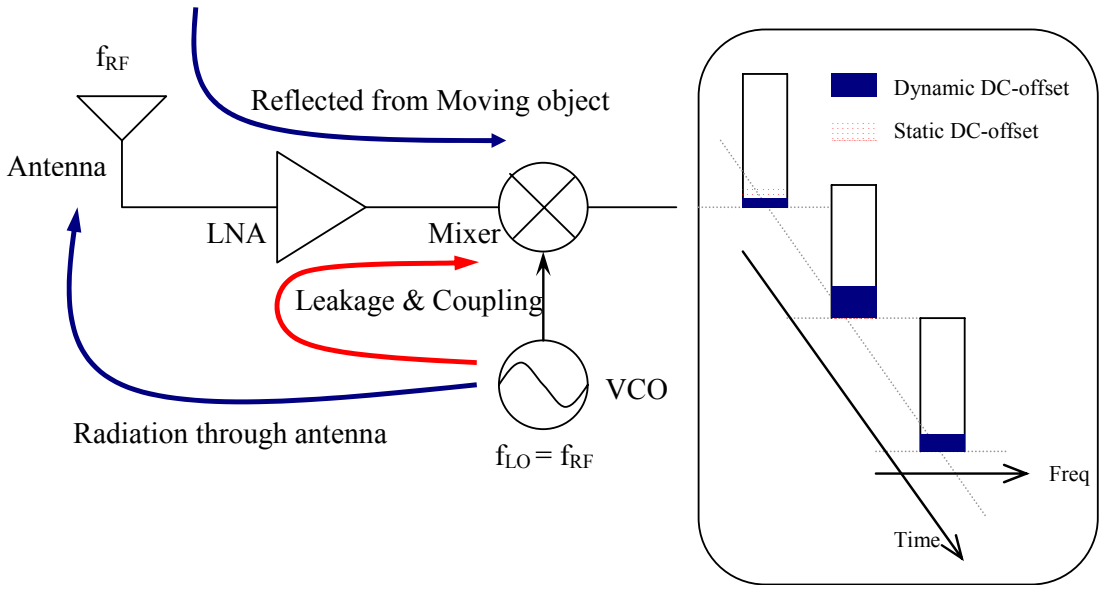
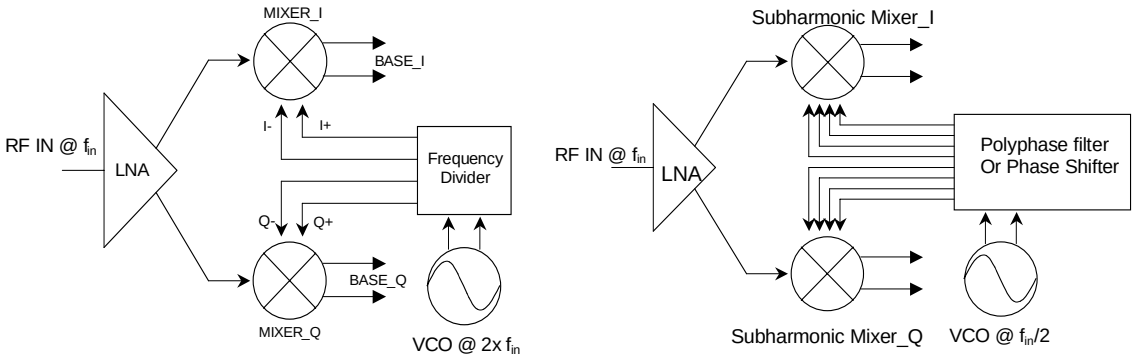


Figure 6.1 DC-offset generation mechanism from a LO signal

Several techniques are available to reduce DC-offset, such as AC-coupling or using a servo amplifier [5] or DSP to cancel the offset. Alternative schemes such as a VCO with a frequency divider or with subharmonic mixing can also be used to reduce DC-offset and in-band LO radiation by moving the LO signal out of the RF frequency band of interest. An example of this approach is shown in Figure 6.2.



(a) (b)

Figure 6.2 (a) A VCO with a frequency divider (b) A VCO with sub-harmonic mixing

The main idea behind these approaches is to use different LO signal and RF signal frequencies, thus eliminating the self-mixing and reducing the DC-offset. In the scheme of Figure 6.2(a), the frequency of a VCO is designed to be twice the RF frequency, and the frequency divider generates a quadrature signal. In the scheme of Figure 6.2(b), the frequency of a VCO is designed at half the RF frequency, and the subharmonic mixer down-converts the input RF signal into the baseband.

When a system requires high output power as seen in Figure 6.3, the high output power of a PA can pull down the frequency of a VCO if the frequency of the VCO is the same as the RF frequency. Even when the VCO frequency is harmonically related to the RF frequency, as in the approaches of Figure 6.2(a) and (b), LO-pulling by a PA and an interaction between a VCO and a PA can happen because of high output power. Therefore, a nonharmonic-related LO signal generation scheme is required to reduce DC-offset and the LO-pulling effect.

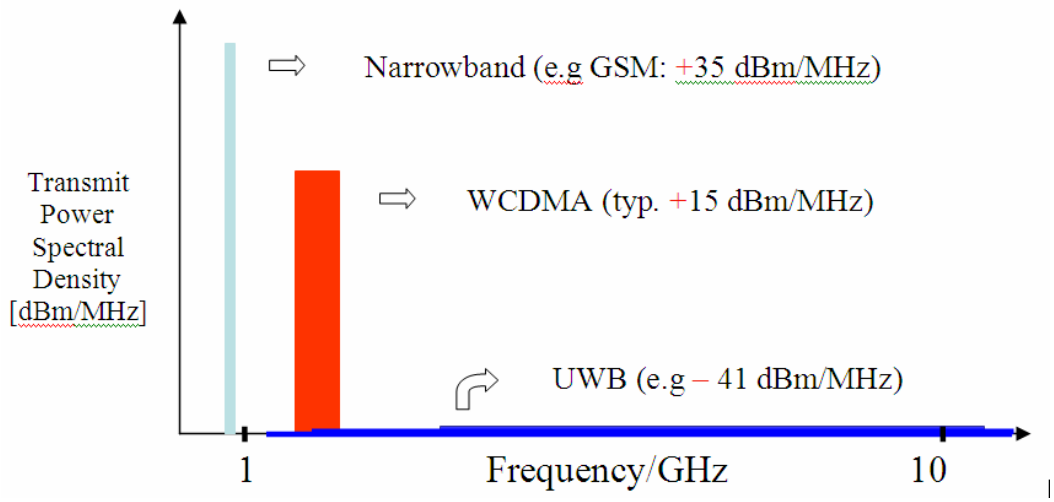


Figure 6.3 Examples of transmit power spectral density for several systems

6.1.2 LO signal generation to generate an accurate quadrature signal

Most current wireless services use QPSK or a variation of this modulation scheme to support their data transfer protocols. This modulation scheme requires I and Q signal separation and demodulation to fully recover the information. Since the conversion process occurs only once at the mixer, the required gain in the RF path increases to meet the system budget, which leads to increased I/Q imbalance. Mismatches between I and Q signals corrupt the down-converted signal constellation, thereby raising the bit error rate.

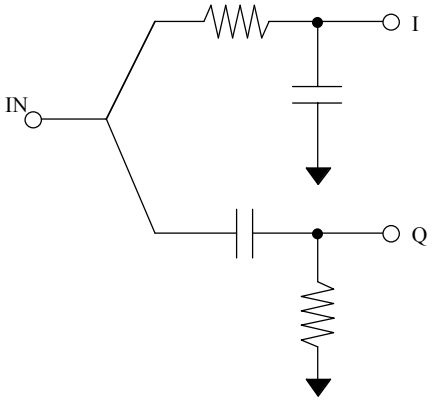
I/Q separation is accomplished by using two down-converters operating in parallel with 90 degrees of phase differentiation. Unfortunately, implementing accurate phase-shifters at a higher frequency becomes a challenge. Heterodyne receivers perform phase differentiation with great accuracy at much lower IF frequencies through simple polyphase circuitry. Phase-shifters used at higher frequencies are either too lossy or suffer from phase and amplitude imbalance generated by parasitics.

For a received-signal defined as $V_{in} = a\cos(\omega_{RF}t) + b\sin(\omega_{RF}t)$, and amplitude and quadrature phase imbalances of ε and θ, respectively, we can describe the baseband I and Q voltages as in Eqn 6.1.

$$V_I(t) = a(1+\frac{\varepsilon}{2})\cos\frac{\theta}{2} - b(1+\frac{\varepsilon}{2})\sin\frac{\theta}{2}$$
$$V_Q(t) = -a(1-\frac{\varepsilon}{2})\sin\frac{\theta}{2} + b(1-\frac{\varepsilon}{2})\cos\frac{\theta}{2} \qquad (6.1)$$

From the equations we deduce that ε appears as a nonunity scale factor in the amplitude, while θ results in cross-talk between the demodulated I and Q waveforms, thus degrading the signal-to-noise ratio (SNR). In practice, for SNR degradation of less than 1 dB in a QPSK signal, ε<1 and θ<1 dB are required.

When an off-chip VCO is used from which the quadrature signals are generated on-chip, RC-CR circuits are commonly used to make two quadrature signals from a single-phase oscillator, as shown in Figure 6.4. In practice, the on-chip R and C tolerances cause an output gain mismatch; thus, it requires two limiters after RC-CR filters to remove the amplitude mismatch. In these limiters, the difference in the phase shift and the AM-PM conversion process can increase the total phase error. Another shortcoming of the RC-CR method is that it needs an undistorted sine wave as input. Distorted input signals (especially harmonics) increase phase error when used as LO signals for mixers. To improve performance, the second harmonic of the input signal can be filtered out by on-chip filters [36]. However, this limits the bandwidth of the quadrature generator. To increase the bandwidth of the filter, several stages with close center frequencies should be staggered. This increases the total loss of the filter drastically.



$$H_I(s) = \frac{I(s)}{IN(s)} = \frac{1}{1+sRC}$$

$$H_Q(s) = \frac{Q(s)}{IN(s)} = \frac{sRC}{1+sRC}$$

Figure 6.4 RC-polyphase filter

Using a divide-by-two stage is another common method to convert a differential phase signal to a quadrature pair. This method is inherently wideband. However, it needs an input LO signal with a perfect 50% duty cycle. In practice, an input signal, which is

usually distorted, especially at high frequencies, can cause phase error. The required 50% duty cycle clock may be generated by another divide-by-two stage, starting with a LO signal with four times the frequency of the desired quadrature signals [48]. A duty cycle corrector or a level locked loop [48] can be used to correct this problem but only at a cost of additional complexity and high power consumption. Extra care should be taken to ensure the symmetry of the layout and the loading of the quadrature paths so that extra phase error is eliminated.

Two VCOs forced to run in quadrature by using coupled transistors can also generate a quadrature signal. Since the frequency of a quadrature VCO is the same as the RF carrier frequency, this approach is poorly suited for a direct conversion receiver. Moreover, this technique requires a trade-off between quadrature accuracy and phase noise. The coupled transistors also decrease the tuning range and increase power consumption. The phase-noise penalty can be circumvented by driving the coupled transistors with additional 90-degree phase shifters [49, 50]. However, an increase in power consumption and a decrease in tuning range remain.

6.2 PROPOSED APPROACH FOR LO SIGNAL GENERATION IN A DIRECT CONVERSION RECEIVER

Usually, the LO signal generation in a direct conversion architecture uses a VCO with a divider to generate a quadrature signal. However, such approach requires a large tuning range for a VCO to cover the frequency range of interest when it is used in multiband application such as GSM/WCDMA. For example, the tuning range requirement for a LO signal for this application is from 1.85GHz to 2.17GHz. When a VCO with a frequency

divider is used to cover this frequency range, the VCO needs to be tuned from 3.7GHz to 4.34GHz. Considering 10% process variation in a standard CMOS process, the required frequency tuning range extends up to 1GHz, which is about 25% of the tuning range at 4GHz. With this large tuning range, a corresponding large tuning gain degrades the phase noise of the VCO because of the AM-FM conversion and also increases power consumption [51]. An increased switching time should be also considered in PLL design. A switched capacitor array can be used to reduce the tuning gain [52], thus alleviating phase noise degradation and long switching time. However, this array adds parasitics and degrades the quality factor of the resonator. As a result, it consumes more power, and the tuning range is reduced as well. This worsens when it involves a standard CMOS process in which only a low Q inductor and lossy capacitors are available. Therefore, there is a need for a compact signal generation method that can relax the large tuning range requirement for the VCO in a standard CMOS process. Also, the generated signal frequency from a VCO should differ from the RF carrier frequency. The concept is shown in Figure 6.5

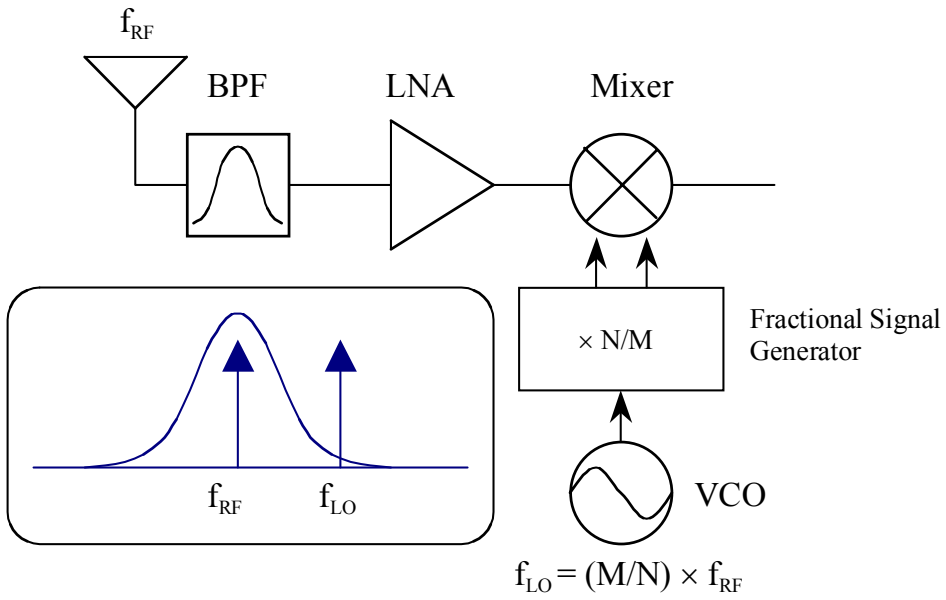


Figure 6.5 A direct conversion receiver with a fractional LO signal generator

6.2.1 Architecture of a fractional LO signal generator

A fractional LO signal generator is an effective way to overcome problems in direct conversion architecture while reducing the tuning requirement of a VCO. In fact, the required LO signal can be generated with proper signal manipulation. The signal from a VCO is fed to a multiplier and a divider. Then a proper LO signal can be generated, but it will be complex and have high power consumption, and added noise. Therefore, it has been only used in a system, such as Bluetooth, that does not require a tight specification [53].

The proposed fractional LO signal generation architecture focuses on reduction of the tuning range requirement for an on-chip CMOS VCO while satisfying all the critical performance factors. The fractional signal generator can reduce the tuning range

requirement of a VCO while maintaining or reducing the phase noise of the VCO with a negligible incremental increase in total power consumption. The architecture is shown in Figure 6.6.

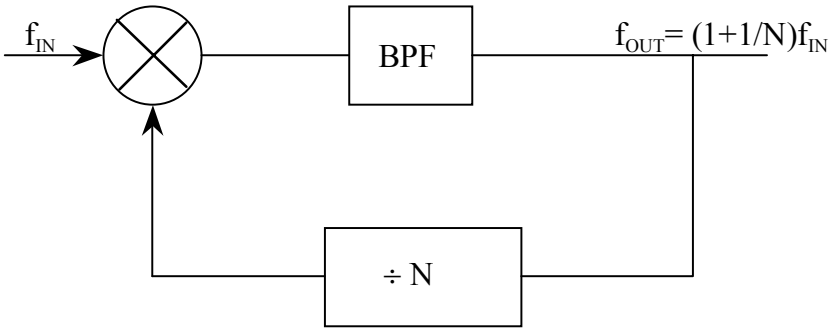


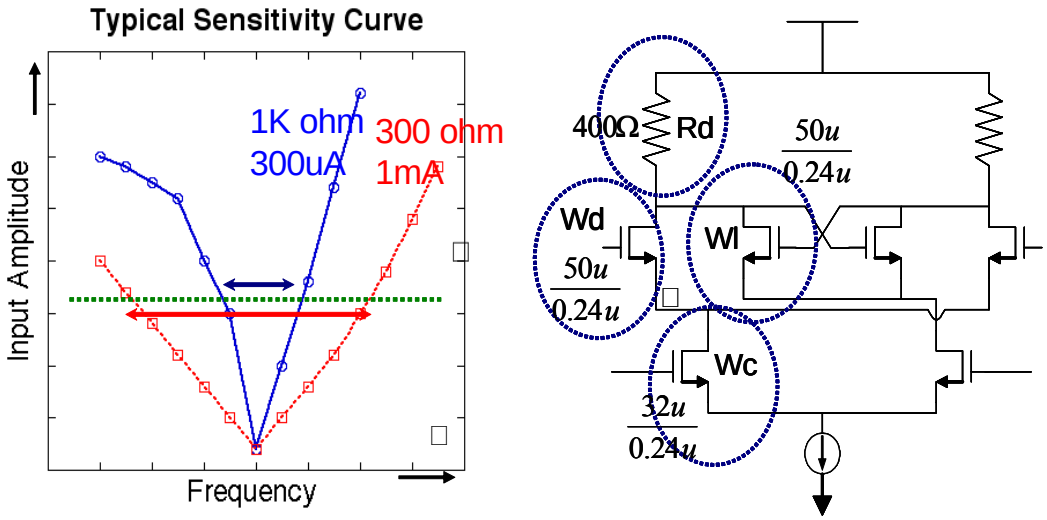
Figure 6.6 Block diagram of the proposed fractional LO signal generation scheme

By incorporating a divider in the feedback path, the frequency of the generated LO signal is the frequency of the input multiplied by N/(N+1). Because the frequency of the VCO is designed to be (N+1)/N, as N increases, the tuning range requirement for the VCO decreases while mitigating DC-offset and LO-pulling problems. The choice of divider topologies can be either a D flip-flop based on current mode logic (CML) or an injection-locked frequency divider.

6.2.2 Design of D flip-flop CML frequency divider

A CML frequency divider is known for its low power consumption and high speed capability, benefits of its reduced voltage swing at the load. There is a trade-off between

the internal voltage swing and the input locking range, and this is controlled by Rd, Wd and Wc.



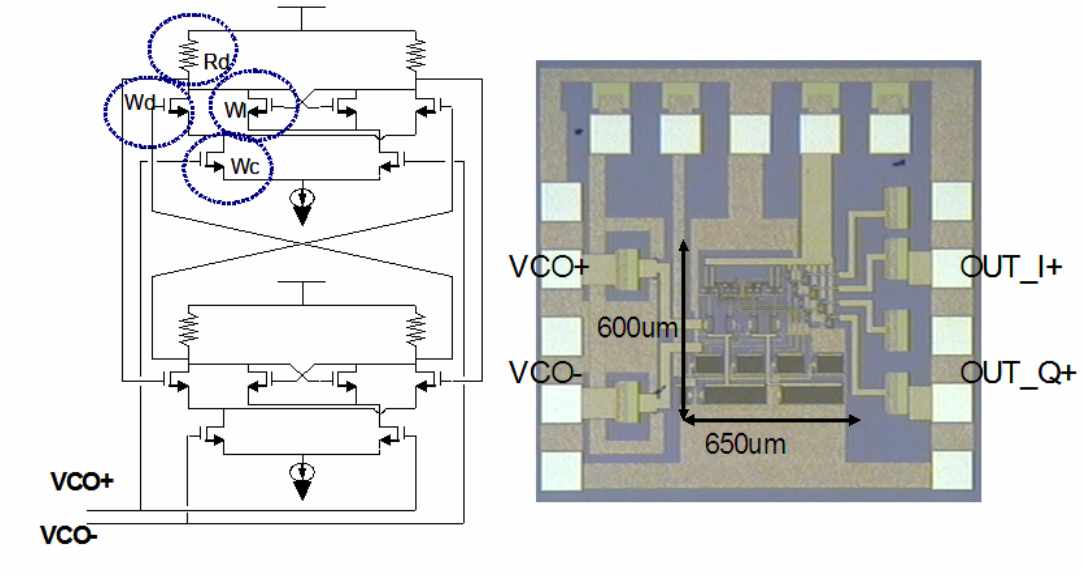
(a) (b)

Figure 6.7 Design principle of a frequency divider (a) Sensitivity curve along with optimization parameters (b) Basic cell of a D-flip flop

In order to ensure that the frequency divider operates with the low input amplitude at the output of a mixer equipped with a bandpass filter in Figure 6.5, the gain from the latch transistor (Wl) and the drive transistor (Wd) should be greater than 1, thus creating a self-oscillation point in the divider [54].

As shown in Figure. 6.7(a), consumption of more current increases the input locking range for the same given voltage swing at the load. Therefore, the frequency divider should be carefully optimized to minimize power consumption and guarantee a large locking range for the input signal. Rd and Wd are selected to have at least 200mV of the internal voltage swing, and Wc is chosen so as to have a large locking range. The

designed basic cell of a D-flip-flop is shown in Figure 6.7(b). The designed frequency divider is fabricated in an 0.25um standard CMOS process. The schematic diagram and photo of the fabricated circuit is shown, respectively, in Figure 6.8(a) and (b). The designed divider consumes 4mA from 2.6V of power supply and operates up to 2.3GHz.



(a) (b)

Figure 6.8 Designed frequency divider (a) Schematic of the divider (b) Photo of the fabricated divider

Figure 6.9 shows the measured performance of the frequency divider. The self-oscillation frequency of the frequency divider is 0.8GHz from the graph. The sensitivity curve shows the operating range for the frequency divider, which can be measured from either a spectrum analyzer or an oscilloscope. Usually the frequency divider is characterized by its sensitivity curve, which gives the minimum input amplitude of the full-rate clock that governs proper operation of the divider's functions versus operation by the applied full-rate frequency [54].

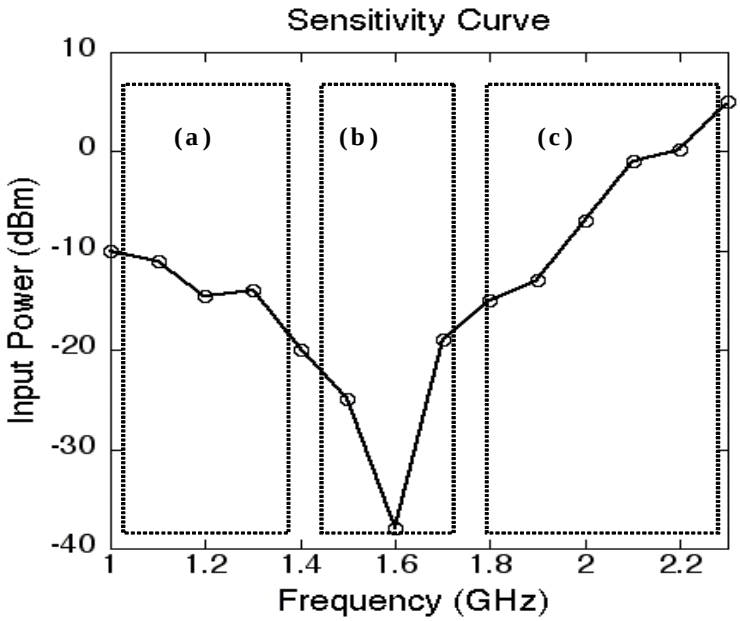


Figure 6.9 Measured sensitivity curve of the CML divider

There are two drawbacks to the use of this divider in the scheme in Figure 6.6. First, the divider is designed to have a self-oscillation point to reduce power consumption. As a result, the frequency response of the divider is very sensitive to load capacitance. Figure 6.6 shows the output of the divider drives into the input of a mixer, which usually has a large input capacitance. Therefore, this reduces the achievable high-frequency operation of the divider. In order to achieve high-frequency operation of the divider, the current consumption should be increased, which leads to more power consumption. Second, the CML divider generates a relatively accurate quadrature signal when the input signal has a perfect 50% duty cycle. Since three different frequency signals (input, output, and the intermediate signal from the divider) are circulating in the architecture in Figure 6.6, the divider cannot generate an accurate quadrature signal, thus causing the architecture to

have poor I/Q mismatch.

6.2.3 Design consideration of injection locked frequency divider

The main concern in a signal generation scheme is to achieve the lowest possible power consumption for implementation of the architecture while achieving the required frequency operation and noise performance. An injection-locked frequency divider (ILFD) has been widely used for synchronization, high gain amplification, and phasing of oscillators in communication electronics and phased-arrays [55]. Recently, it has been used in a prescaler [56], for quadrature signal generation [57] and in a frequency synthesizer [58]. In a cross-coupled differential oscillator, the common mode voltage of the circuit actually oscillates at twice the oscillation frequency, which originates from the rectifying action of the two MOS switches. Therefore, it is a natural candidate to realize a divide-by-two function, as shown in Figure 6.10.

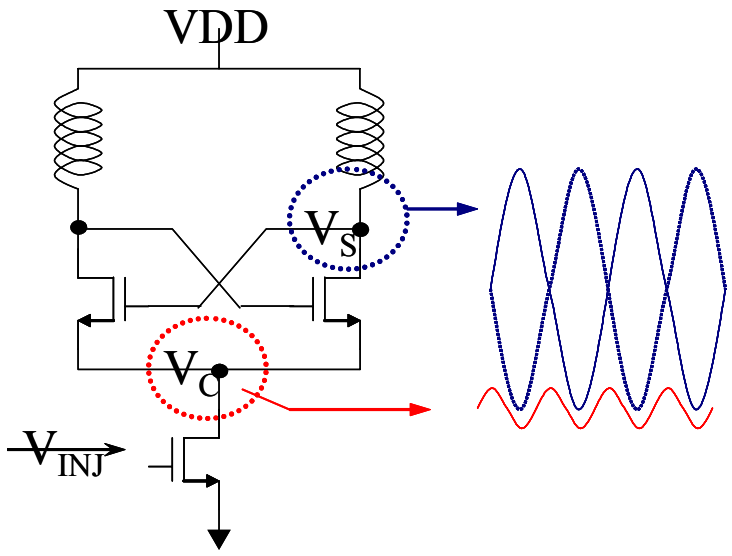


Figure 6.10 Principle of an injection-locked frequency divider (ILFD)

Because the ILFD is actually an oscillator, the circuit needs very little power to operate properly compared with a CML divider. The self-oscillation frequency of the ILFD is represented by $f_o = 1/2\pi\sqrt{LC}$, where L and C are total inductance and capacitance, respectively, seen at the load. Since any added parasitic at the load of the ILFD can be incorporated into the design, the design can achieve high frequency operation with low power consumption. Furthermore, the design can be extended to generate an accurate quadrature signal. One of the disadvantages resident in a ILFD is its limited input locking range because of the tuned nature of the circuit.

The input locking range, φ, can be expressed as in Eqn 6.2 according to the [59].

$$\varphi \cong \left| \frac{H_o V_i}{Q} \right| \qquad (6.2)$$

in which *Vi* is the incident amplitude of an ILD, *Ho* is the impedance of the resonator, and *Q* is a quality factor of the inductor. The locking range can be enhanced by increasing either *Ho/Q* or the incident amplitude *Vi*. In the proposed scheme, the frequency of the incident signal to the ILD is the same as the RF carrier frequency. As a result, there is a limit for the incident amplitude *Vi* to minimize the DC-offset. *Ho/Q* can be increased by using low Q inductor with large inductance in the design.

6.3 CIRCUIT IMPLEMENTATION OF FRACTIONAL SIGNAL GENERATOR

Because an ILFD can perform a dividing function, especially in high frequencies, without adding much complexity and power consumption [59], an ILFD is used as a divider in the scheme. The disadvantage of an ILFD is its limited locking range. The /use of an ILFD in the design of a fractional signal generator constitutes the bottleneck for the generator to work in a wideband application. The problem can be solved by incorporating

a tuning element in the ILFD, which can be varied with the control voltage for a VCO as shown in Figure 6.11.

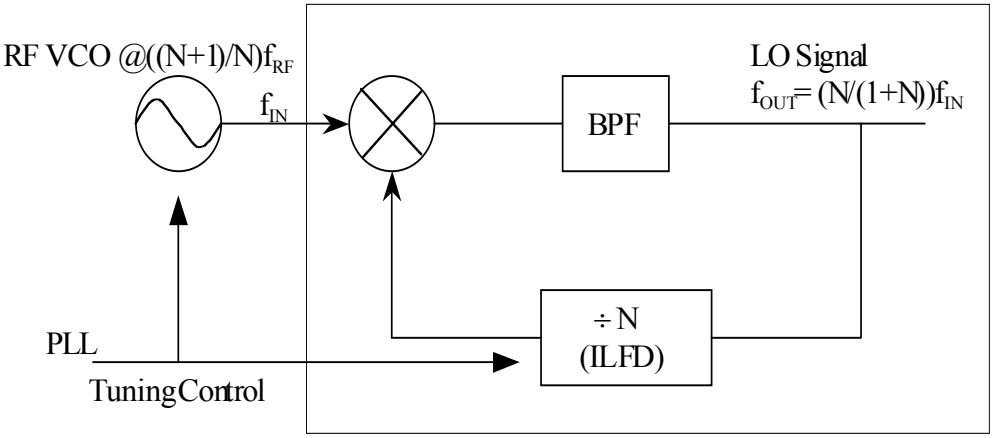


Figure 6.11 Block diagram of a proposed circuit implementation.

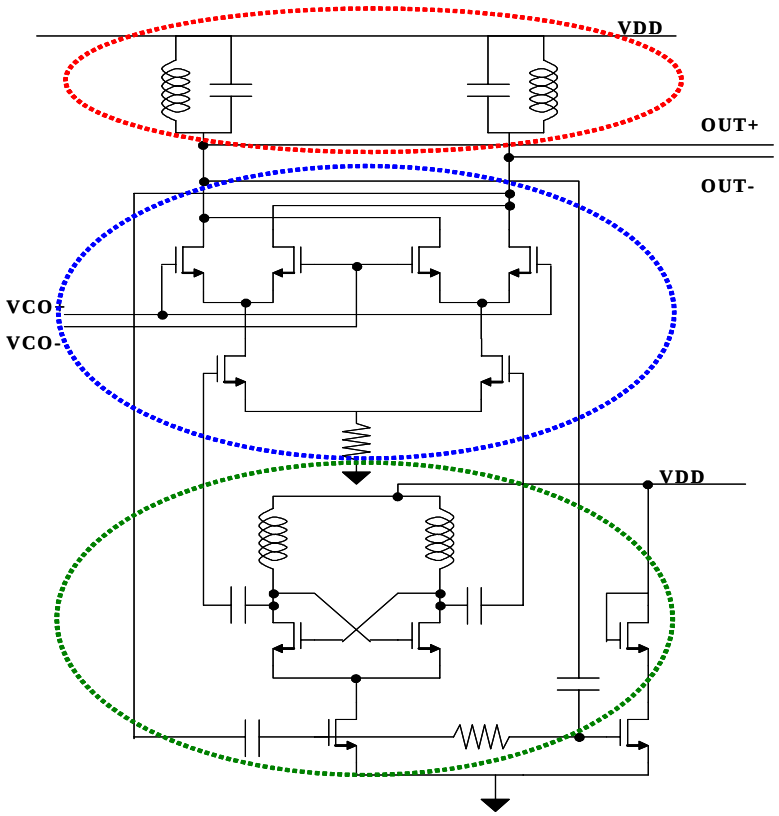


Figure 6.12 Schematic diagram of the proposed fractional signal generator.

The schematic of the proposed fractional signal generator is shown in Figure 6.12. A Gilbert-cell is used as a mixer equipped with a bandpass load to simplify the implementation of the architecture in Figure 6.11. The current flowing in the mixer has energy at odd harmonic frequencies because of the switching action in the VCO-driven stage. The current is changed into voltage at the load, which is filtered out through the bandpass filter. One of the outputs of the mixer is connected to the input of the ILFD. In order to make sure that the output sees the same amount of parasitic, the other output of the mixer is connected to a dummy gate. A cross-coupled differential pair is used as the ILFD. Because of the large voltage swing of the ILFD to the input of the mixer in Figure

6.12, the required conversion gain in the mixer can be obtained with low power consumption. Also, it reduces the required input voltage swing from a VCO. Therefore, by using the ILFD in the feedback path, power consumption in the mixer and the divider can be reduced substantially.

6.3.1 Design considerations for operating range

The main concerns in the proposed LO signal generation scheme are low power consumption, range of operation and the noise performance of the architecture. The ILFD used in the scheme can perform a further division function with little additional power consumption. In this work, a divider-by-two is implemented in the fabrication to test the feasibility of the scheme.

The disadvantage of an ILFD is its limited locking range. Even though a control scheme is used in Figure 6.11, the locking range of the ILFD should be designed large enough to accommodate the process variations of CMOS technology. A cross-coupled differential pair with an input transconductance stage is used as the ILFD. The locking range of the divider is proportional to the voltage swing at the node, as seen in Figure 6.10. A small device is preferable because it can efficiently amplify the input voltage and modulate the voltage swing at the node. The device size for the transconductance stage in the ILFD is optimized to achieve a divide-by-two function over a large locking range.

6.3.2 Design consideration for noise performance

Since the phase noise of an ILFD tracks the phase noise of an input signal within its effective loop bandwidth when the ILFD is locked to the input signal, the noise

performance of the proposed generator is determined primarily by the noise performance of the ILFD. The loop bandwidth is related to the locking range [60]. The expression of the locking range is already illustrated in Eqn. 6.2.

From Eqn. 6.2, we can deduce that the phase noise of the ILFD is inversely proportional to the locking range, considering the fact that the phase noise improves along with the increment of quality factor of the resonator. Since the phase noise of the ILFD tracks the phase noise of the injected input signal, extra care should be taken to ensure that the phase noise of the ILFD is low enough to satisfy the specifications of the target communication system at the far offset frequency. One way to overcome this issue is to increase the loop bandwidth of the ILFD. By increasing loop bandwidth, fast locking time as well as low noise performance can be obtained. A large sized inductor with a low quality factor can increase the loop bandwidth as well as the locking range. An 11nH of inductor is designed for the ILFD in Figure 6.12 using ASITIC with an intentionally low quality factor to increase the locking range. The designed inductor achieves Q of 3 around 1GHz.

Simulated phase noise of each signal in Figure 6.12 is shown in Figure 6.13. It shows that the phase noise of the fractional signal generator tracks the phase noise of the input referenced VCO within the loop bandwidth. The phase noise of the fractional signal generator tracks the phase noise of the ILFD outside of the loop bandwidth. Therefore, the loop bandwidth must be designed to achieve a low noise floor, which can be tolerated in the target application systems.

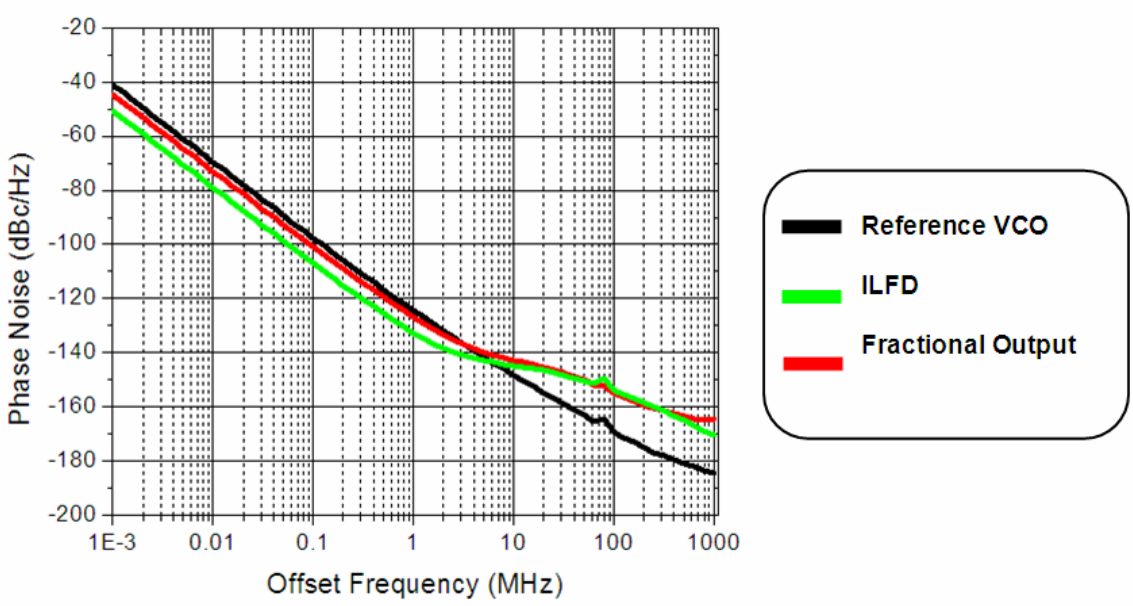


Figure 6.13 Simulated phase noise of reference VCO, ILFD, and the output of fractional signal generator

6.4 MEASURED RESULTS OF THE FRACTIONAL SIGNAL GENERATOR

The design is fabricated in a 0.18um standard CMOS process. The process has five metal layers with less than 1um thickness of top metal. The photo of the fabricated chip is shown in Figure 6.14. The size of the fabricated fractional signal generator is 905um x 1012um including pads.

The ILFD and the fractional signal generator are measured using 83650A synthesized sweeper and 8565E spectrum analyzer with phase noise measurement setup.

The measured tuning range of the ILFD performing a divide-by-two function is illustrated in Figure 6.15, along with the locking range. The locking range of the ILFD is between 480MHz and 630MHz when 0dBm of signal is injected. As shown in Figure 6.15, the locking range increases as the varactor gain increases.

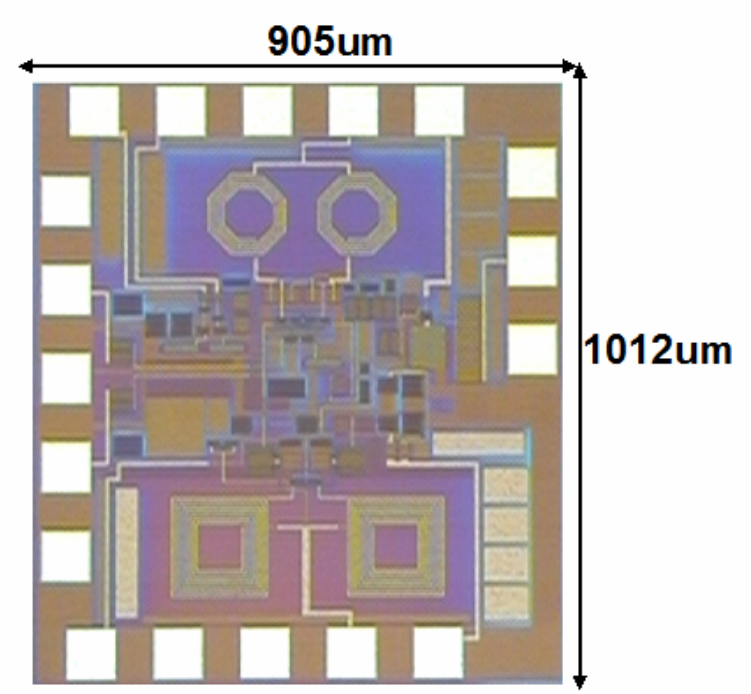


Figure 6.14 Photo of the fabricated fractional signal generator.

Figure 6.16 shows the phase noise of the free running ILFD and the phase noise of the ILFD when it is locked to its fundamental oscillation frequency. Noise improvement can be seen over 10MHz frequency offset even though further improvement is not shown because of the dynamic range limit of the measurement system.

Figure 6.17 shows the operating frequency range of the generator along with the control voltage. For the input signal, a locking range of 165MHz is obtained and 110MHz is obtained for the output signal. With the tuning control, when the input is applied from 2.29 GHz to 3.29 GHz, the output is generated from 1.53GHz to 2.19GHz, covering the range required for GSM/WCDMA dual band application.

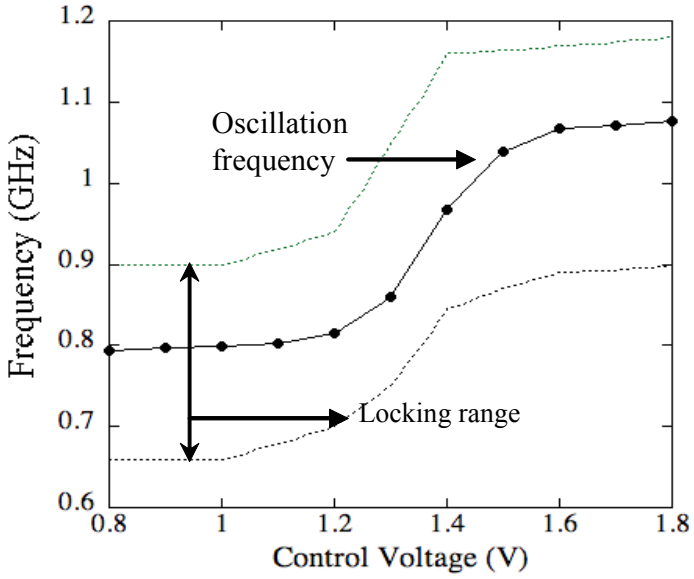


Figure 6.15 Measured tuning and locking range of the ILFD.

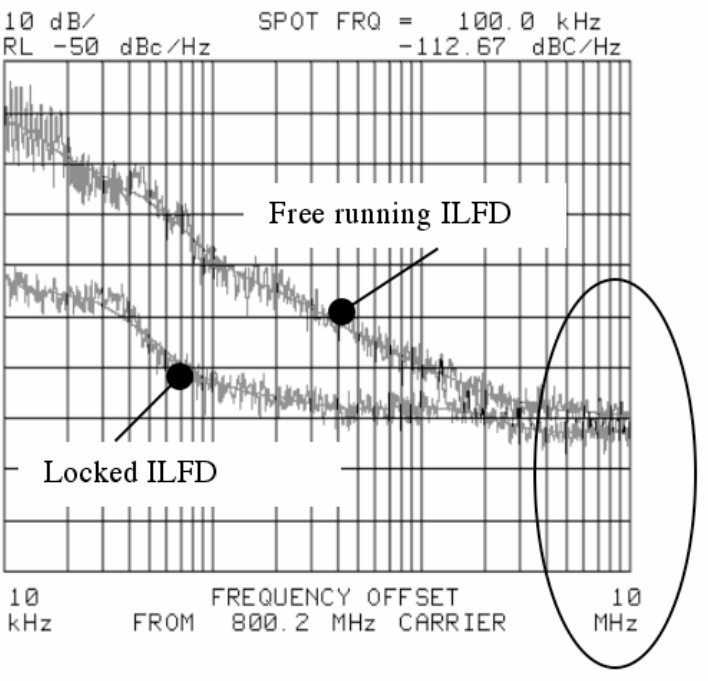


Figure 6.16 Locking bandwith of the designed ILFD

The output spectrum of the generator is shown in Figure 6.18. The leakage from the ILFD and the injected signal source are measured along with the desired output signal. The leakage suppression is more than 35dBc, compared with the desired output signal. Noise performance of the generator is shown in Figure 6.19. The generator reduces the phase noise of the input signal as much as 3.5dB within the loop bandwidth.

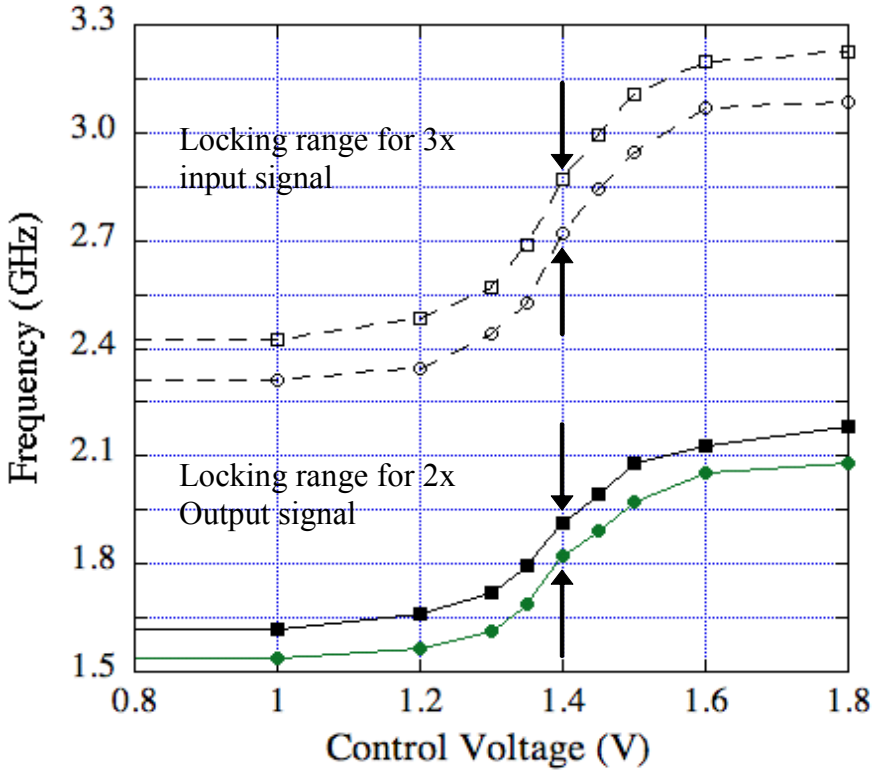


Figure 6.17 Measured tuning and locking range of the fractional signal generator for its input and output signal.

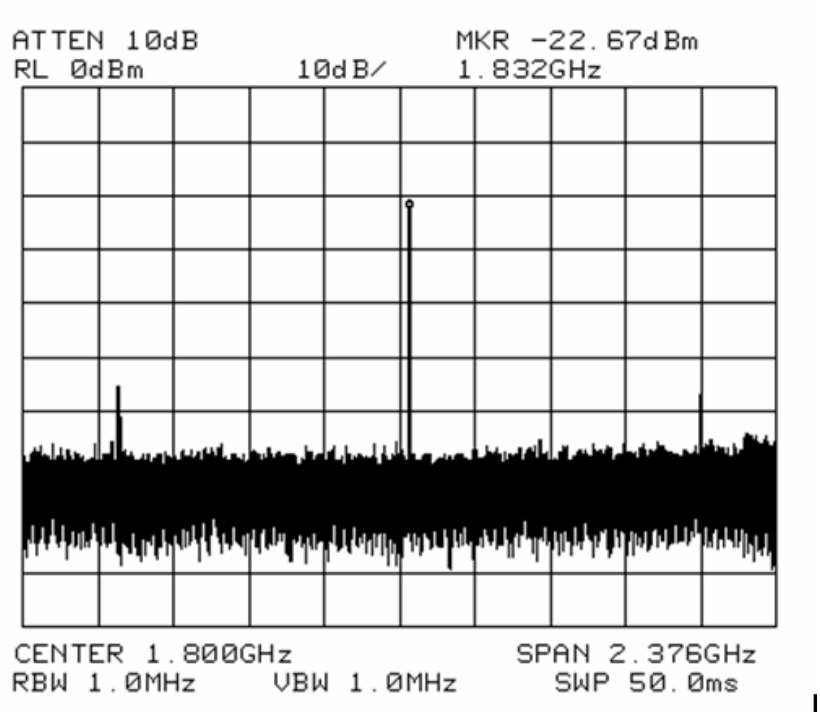


Figure 6.18 Output spectrum of the fractional signal generator along with 1x and 3x leakages caused by ILFD and injection source.

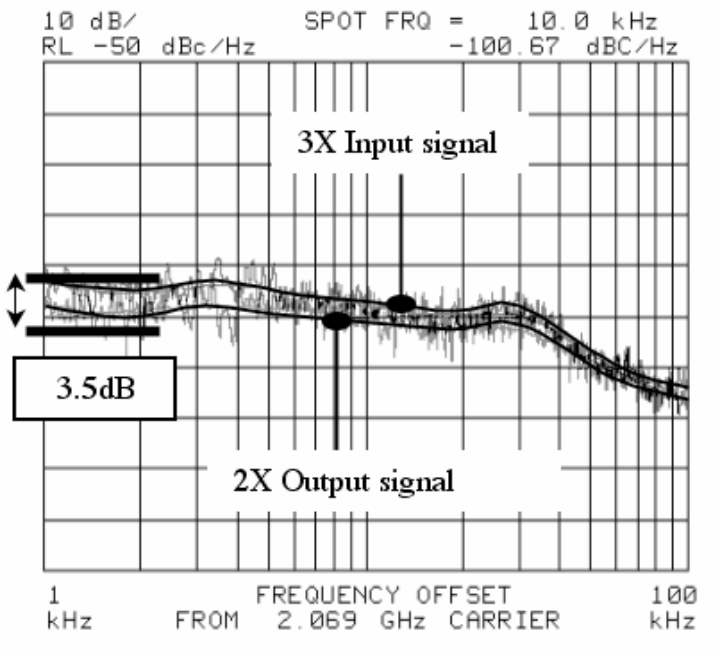


Figure 6.19 Phase noise of 2X output signal with 3X input signal

The voltage swing at the load of the generator is designed to be low for its use in a direct conversion architecture and to ensure the good noise performance in the generator. Measurement shows a 200mVpp voltage swing at the load. Because of the low voltage swing, the locking range of the fractional signal generator is reduced compared with that of the standalone ILFD test structure. However, the low voltage swing also reduces LO-RF leakage in a RF mixer when it is applied.

6.5 SUMMARY

In this chapter, a compact implementation for a fractional signal generator is proposed that can reduce the tuning range requirement of a VCO and simultaneously alleviate the DC-offset problem in direct conversion architecture with low power consumption. The designed and fabricated CMOS circuit achieves low noise floor of –100dBc at 10KHz offset frequency. The design considerations for the proposed fractional signal generator are discussed. The generator covers the frequency range for GSM/WCDMA dual band application. The design can be extended for high frequency applications without consuming extra power because of the low power characteristic of the ILFD.

CHAPTER VII

CONCLUSION AND FUTURE WORK

7.1 TECHNICAL CONTRIBUTIONS AND IMPACT OF THE DISSERTATION

The increasing demands of customers for higher data rate with more convenient platforms are forcing the development of new applications such as the UWB system and multiband, multimode applications. Such systems require RF front-end to support a wideband signal, whereas traditional wireless systems only have to deal with a narrowband signal. Therefore, a conventional design technique as well as RF front-end architecture for narrowband applications should be modified and improved to solve obstacles in implementing RF front-end for emerging wideband applications.

In commercial applications the cost of implementing those systems is a critical parameter to decide whether or not they can be successful in the consumer market. Considering the SOC approach that permits a smaller and lower cost solution, efforts to accommodate the current trends of wideband systems should be exercised on silicon-based technologies such as the CMOS and SiGe BiCMOS processes. Since the target systems have mobile wireless communication applications as their goal, power consumption needs to be minimized to prolong battery life.

This dissertation addresses various design aspects of the RF components for the design of wideband applications. The research mainly focuses on developing state-of-the-art ICs and innovative architecture to provide low cost, low power consuming solutions to the present problems associated with wideband applications. As an effort to find solutions,

this dissertation includes a vast scope of research begins with understanding the system under consideration and progresses to the details of the manufacture and operation of transistors. Research has been performed on two nominal wideband systems, which are the UWB system and the GSM/WCDMA dual-band application.

The recent actions of the FCC regarding frequencies between 3GHz and 10GHz for UWB applications has increased an interest in this band and its various applications. Two systems are proposed for the use of the UWB frequency range, yet very little information is available on the implementation of the RF front-end for those systems because both are in their early stage of product development. Chapter Two briefly depicts the history of the UWB concept and compares these two systems from the perspective of RF front-end implementation. Besides the traditional circuit design specifications — such as noise, gain, linearity and power consumption — this dissertation identifies the group delay variation as a critical design parameter in the implementation of UWB RF front-end. In the absence of any theoretical analysis on controlling the group delay variation of an LNA, a technical analysis has been performed to optimize gain, noise, linearity, and group delay performance of an LNA for wideband operation while also consuming very little power. As a result, we determined and demonstrated experimentally that low base inductance in the design of SiGe HBT LNA is beneficial to achieve low group delay variation while maintaining a low noise figure. Furthermore, the analysis performed in the design of the LNA can give significant insight into the process aspect, thus enabling the development of an optimum process that will be properly positioned for the design of wideband RF components.

The main challenges in implementing an RF front-end for the UWB system are to

achieve the very wideband operation while satisfying stringent specifications for gain, noise, and linearity and minimizing DC power consumption. Since achieving wideband operation and good linearity are related to current consumption, it is difficult to satisfy those conditions and also have low DC power consumption. A full-band direct conversion receiver is designed for the UWB multiband OFDM system in SiGe HBT BiCMOS process, and we demonstrated that the required performance in the RF receiving path for the system can be achieved with a very low power consumption of 30mW. This figure of merit (FOM) can set the performance criteria for the development of future UWB receivers.

Besides the UWB system, the current efforts to integrate several wireless applications into a single mobile system posed several challenges to the design of a LO signal generation. Because CMOS devices have poor flicker noise performance and higher flicker corner frequency, research has been performed especially on the design of the LO signal generation using a standard CMOS process. Two wideband VCOs have been designed in 0.25um standard CMOS process achieving a tuning range of more than 20%. AM-FM noise conversion in high gain varactors has been identified as a dominant performance degradation factor in the design of a wideband VCO. This is demonstrated experimentally by comparing the design and measurement of two VCOs. With a tail current source, the phase noise of the wideband VCO is degraded by AM-FM noise conversion because of the high varactor gain. However, if a current source is omitted, the performance of the VCO depends heavily on the process variations. The power consumption of such a VCO can vary up to two times over the process corners. In order to reduce the tuning burden of the wideband VCO, and also the DC-offset and LO-pulling

problems in a direct conversion receiver, a fractional LO signal generator is proposed and designed in a 0.18um standard CMOS process. The performance of the generator is experimentally demonstrated for GSM/WCDMA dual-band application. A qualitative analysis was performed on its frequency range of operation, power consumption, locking range and noise performance. As a result, we identified that a large value of an inductor in the design of an injection-locked frequency divider determines the frequency range of operation, the locking range and the noise performance of the fractional signal generator. Through simulations, we showed that the phase noise of the fractional signal generator tracks the phase noise of the input reference signal within the loop bandwidth, and follows the phase noise of an injection-locked frequency divider outside the loop bandwidth. Hence, the loop bandwidth is a critical design parameter of a fractional signal generator in order for such a generator to be used in wireless systems. The measured output of the generator shows that other spurious signals are rejected by more than 35dB, which is a comparatively better performance that is reported in [53]. Also, we demonstrated experimentally that the phase noise of the fractional signal generator can reduce the phase noise of the input reference signal by 3.5dBc/Hz.

Finally, the contributions of this dissertation can be summarized as follows:

1. The RF front-end design, including the RF receiver and the LO signal generator, is discussed for wideband applications such as UWB and a GSM/WCDMA dual-band system on SiGe HBT BiCMOS and CMOS processes.

2. A theory to control group delay variation is proposed and demonstrated experimentally through the design and measurement of a UWB LNA.

3. The analysis performed on the group delay variation, noise figure and linearity of the UWB LNA reveals that low base inductance is beneficial to achieve low group delay variation and a low noise figure over the UWB band. Secondly, the input capacitance of a SiGe HBT device should be minimized to achieve a flat group delay in the higher frequency range of operation. Thirdly, because there are trade-offs between linearity, noise and group delay performance of the LNA, depending on the value of source impedance, a low loss impedance transformer can be used to transform the high impedance of a wideband antenna to the optimum source impedance.

4. A 3GHz-10GHz UWB direct conversion receiver is demonstrated with very low DC power consumption of less than 30mW.

5. 4GHz CMOS VCOs are designed and compared. The phase noise performance of the VCOs with wide tuning ranges are presented. The critical noise source that affects the phase noise of wideband VCOs is identified.

6. A CMOS fractional LO signal generator is presented as a promising solution for the implementation of a direct conversion scheme for GSM/WCDMA dual-band applications.

7.2 SCOPE OF FUTURE RESEARCH

In this dissertation, research focused on the implementation of a UWB receiver. Even though we achieved a wide frequency operation with low DC power consumption, another challenge remains for LO signal generation for the UWB MB-OFDM receiver. The direct conversion architecture requires that the LO signal cover from 3GHz to 10GHz. Since this vast frequency tuning range cannot be achieved by a single VCO, a new method should be developed. Another problem in implementing LO signal generation in the receiver is that the switching time allowed for the LO frequency to

choose a band should be within a guard interval of 9.5ns. The design of a frequency synthesizer to satisfy this very short settling time is quite challenging, and this is one of the research topics under active pursuit.

A fractional LO signal generator has been demonstrated for the GSM/WCDMA dual-band application. The design can be extended to generate a quadrature signal by incorporating a quadrature injection-locked frequency divider. It would be very interesting to compare the extended design to other methods in terms of I/Q imbalance.

APPENDIX A

Using linear two-port noise theory, we can convert the noise model in Fig.2 into an equivalent input noise current generator, $v_n(t)$ and an input voltage noise generator, $i_n(t)$ with noiseless 2-port model [61].

The corresponding power spectral densities (PSDs) are defined by

$$S_{vn}(f) = \lim_{\tau \to \infty} \frac{2\overline{|v_n(f)|^2}}{\tau} \qquad \text{(A.1)}$$

$$S_{in}(f) = \lim_{\tau \to \infty} \frac{2\overline{|i_n(f)|^2}}{\tau} \qquad \text{(A.2)}$$

where $v_n(f)$ and $i_n(f)$ is the Fourier transforms for noise voltage and current defined by [61]

Using the Y-parameter equation described in [27], the expression for S_{vn}, S_{in} can be derived as follows

Suppose $Z_L >> R_F$,

$$S_{vn} = \frac{4kTg_m^2}{g_o^2}\left(\frac{1}{2g_m} + \frac{g_f}{g_m} + r_b\right) \qquad \text{(A.3)}$$

$$S_{in} = \frac{2qI_c}{g_o^2}\left(\frac{g_o^2}{\beta} + (1+\frac{2}{\beta})g_f^2 + (\omega C_i)^2\right) \qquad \text{(A.4)}$$

$$S_{in \cdot vn^*} = 2qI_c\left(\frac{g_f + \frac{g_m}{\beta} + j\omega C_i}{g_o^2}\right) \qquad \text{(A.5)}$$

where $C_i = C_{be}+C_{bc}$, $g_f = 1/R_F$, $g_o = g_m - g_f$

From the above equations, we can derive the following equations

$$R_n = \frac{S_{vn}}{4kT} = \frac{g_m^2}{g_o^2}\left(\frac{1}{2g_m} + \frac{g_f}{g_m^2} + r_b\right) \qquad \text{(A.6)}$$

$$G_{s.opt} = \sqrt{\frac{S_{in}}{S_{vn}} - \left[\frac{\mathrm{Im}(S_{in\cdot vn^*})}{S_{vn}}\right]^2}$$
$$= \sqrt{\frac{g_m}{2g_o^2 R_n}\left[\frac{g_o^2}{\beta} + \left(1+\frac{2}{\beta}\right)g_f^2\right] + \frac{g_m(\omega C_i)^2}{2g_o^2 R_n}\left(1 - \frac{g_m}{2g_o^2 R_n}\right)} \qquad \text{(A.7)}$$

$$B_{s.opt} = -\frac{\mathrm{Im}(S_{in\cdot vn^*})}{S_{vn}} = -\frac{g_m(\omega C_i)}{2g_o^2 R_n} \qquad \text{(A.8)}$$

Using (A.6)-(A.8), NF_{min} is expressed as follows

$$NF_{\min} = 1 + 2R_n\left(G_{s.opt} + \frac{\mathrm{Re}\left(S_{in\cdot vn^*}\right)}{S_{vn}}\right)$$
$$= 1 + \frac{g_m}{2g_o^2 R_n}(g_f + \frac{g_m}{\beta})$$
$$+ \sqrt{\frac{2g_m R_n}{g_o^2}\left[\frac{g_o^2}{\beta} + \left(1+\frac{2}{\beta}\right)g_f^2\right] + \frac{2g_m R_n(\omega C_i)^2}{g_o^2}\left(1 - \frac{g_m}{2g_o^2 R_n}\right)} \qquad \text{(A.9)}$$

Suppose $r_b >> 1/(2g_m)$, NF_{min} can be expressed as follows.

$$NF_{\min} \cong 1 + \frac{g_m}{g_o^2}\left(g_f + \frac{g_m}{\beta}\right) + \frac{g_m^2}{g_o^2}\sqrt{2g_m r_b}\sqrt{\frac{1}{g_m^2}\left(\frac{g_o^2}{\beta} + g_f^2\right) + \left(\frac{f}{f_T}\right)^2} \qquad \text{(A.10)}$$

APPENDIX B

From Eqn.3.24, $G_1(s)$, $G_2(s_1,s_2)$, $G_3(s_1,s_2,s_3)$ can be expressed as follows [29].

$$G_1(s) = g_m C_1(s) \tag{B.1}$$

$$G_2(s_1, s_2) = g_m C_2(s_1, s_2) + \frac{I_c}{2V_T^2} C_1(s_1) C_1(s_2) \tag{B.2}$$

$$G_3(s_1, s_2, s_3) = g_m C_3(s_1, s_2, s_3) + \frac{I_c}{6V_T^3} C_1(s_1) C_1(s_2) C_1(s_3) + \frac{I_c}{V_T^2} \overline{C_1 C_2} \tag{B.3}$$

Using a technique known as compact modified nodal analysis (CMNA) [27], $C_1(s)$, $C_2(s_1,s_2)$, $C_3(s_1,s_2,s_3)$ can be obtained as follows. r_b is ignored because its effect is negligible.

$$Z_g(s) = R_s + sL_B \tag{B.4}$$

$$Z_L(s) = R_L + sL_L \tag{B.5}$$

$$Z_F(s) = R_F + (1/sC_{bc}), \;\; Y_F = 1/Z_F \tag{B.6}$$

$$C_1(s) = \frac{1}{1 + sZ_g(C_{dif} + C_j) + 1/r_\pi + Y_F + \dfrac{g_m - Y_F}{1 + \dfrac{1}{Y_F Z_L}}} \tag{B.7}$$

$$C_2(s_1+s_2) = -C_1(s_1+s_2)C_1(s_1)C_1(s_2)\frac{I_c}{2V_T^2} \times\left[\frac{Z_g(s_1+s_2)}{\beta}+(s_1+s_2)\tau_f Z_g(s_1+s_2)+Z_x(s_1+s_2)\right] \quad \text{(B.8)}$$

where $Z_x = \dfrac{Z_g Z_L}{R_F + Z_L}$,

$$C_3(s_1,s_2,s_3) = -\frac{C_1(s_1+s_2+s_3)I_c}{6V_T^3}\left(C_1(s_1)C_1(s_2)C_1(s_3)+6V_T\overline{C_1C_2}\right) \times\left[\frac{Z_g(s_1+s_2+s_3)}{\beta}+(s_1+s_2+s_3)\tau_f Z_g(s_1+s_2+s_3)+Z_x(s_1+s_2+s_3)\right]$$

(B.9)

$$\overline{C_1C_2} = \frac{1}{3}\left(C_1(s_1)C_2(s_2,s_3)+C_1(s_2)C_2(s_1,s_3)+C_1(s_3)C_2(s_1,s_2)\right)$$

(B.10)

By substituting (B.7)-(B.10) into (B.1)-(B.3), we obtain the following equations.

$$G_1(s) = \frac{g_m}{1+\left(R_s+sL_B\right)\left(s(C_j+C_d)+r_\pi+g_F+\dfrac{g_m-g_F}{1+\dfrac{1}{g_F Z_L}}\right.}$$

(B.11)

$$G_2(s_1,s_2)=\frac{V_T}{2I_C^2}G_1(s_1)G_2(s_2)G_1(s_1+s_2)$$
$$\times\left[1+(s_1+s_2)C_jZ_g(s_1+s_2)+\frac{Z_g(s_1+s_2)}{Z_F(s_1+s_2)+Z_L(s_1+s_2)}\right] \quad \text{(B.12)}$$

$$G_3(s_1,s_2,s_3)=\frac{V_T}{3I_C^3}G_1(s_1+s_2+s_3)\left[3I_C\overline{G_1G_2}-G_1(s_1)G_2(s_2)G_3(s_3)\right]$$
$$\times\left[1+(s_1+s_2+s_3)C_jZ_g(s_1+s_2+s_3)+\frac{Z_g(s_1+s_2+s_3)}{Z_F(s_1+s_2+s_3)+Z_L(s_1+s_2+s_3)}\right]$$

(B.13)

$$\overline{G_1G_2}=\frac{1}{3}\left(G_1(s_1)G_2(s_2,s_3)+G_1(s_2)G_2(s_1,s_3)+G_1(s_3)G_2(s_1,s_2)\right)$$

(B.14)

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Vita

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